D2.4 Experimental results and validation of lab-scale power converters prototypes

Reinventing High-performance pOwer converters for heavy-Duty electric trAnSport

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v.7	20-01-2025	David Lumbreras	Modified chapter 4
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DISCLAIMER

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EXECUTIVE SUMMARY

This D2.4 document provides a comprehensive report on the activities related to the experimental validation of lab-scale power converter prototypes. It includes an analysis of the current standards for power converter testing, drawing on publicly available sources and the expertise of RHODaS partners.

The document also proposes a detailed test plan for High Power Converters (HPC), which are based on Low Power Converter modules. This plan encompasses electrical tests for both Low Voltage (LV) and High Voltage (HV) parts, as well as environmental, mechanical, and safety tests. Additionally, the document reports on laboratory tests to verify basic parameters of Low Power Converters (LPC), such as efficiency, distortion, and Common Mode Voltage (CMV).

The analysis highlights the absence of comprehensive standards for inverter testing, necessitating the search for relevant documents from various testing fields. Due to the high voltage levels considered in the DC/AC converter, of at least 1000 VDC Bus, it is necessary the adaptation of research methodologies in cases where direct references are lacking. This process requires substantial knowledge and experience in test systems and application of standards.

The conclusions drawn from these activities are expected to support future design, optimization and recommendations, focusing on further improvements in power converters and the use of standards specifically adapted for them in automotive applications.

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1 INTRODUCTION

1.1 DESCRIPTION OF THE DOCUMENT AND PURSUE

This report analyzes various standards that may apply to the converters developed within the RHODaS project. As the project involves a prototype and introduces novel technology, certain existing standards may not be directly applicable and may require modification to accommodate the developed technology.

Additionally, the document details the experimental results obtained from low-power converters. These results are used to validate the work conducted during WP2. This validation is extremely important since the tested protection algorithms, operating modes, and modulation techniques will be applied to the high-power converter to be validated in WP5.

Finally, based on the experimental results and existing standards, this deliverable develops a test plan for the high-power converter developed in the project.

1.2 WPS AND TASKS RELATED WITH THE DELIVERABLE

This deliverable refers to Task 2.8 included in WP2: Design of electric and electronics components.

2 REVISION AND ANALYSIS OF EXISTING STANDARDS

This section presents a comprehensive review and analysis of existing standards pertinent to the new generation of electric vehicle converters developed in the RHODaS project. Since the developer converters are prototypes and introduce novel technologies, current standards may not fully encompass their unique features and requirements. Consequently, some standards may require adaptation or modification to align with the innovations we have implemented.

The analysis delves into various standards across automotive, railway, and industrial sectors, with a particular focus on those related to inverter and electrical component testing. Notably, harmonised standards and tests such as EN 62477 are examined.

2.1 EXISTING STANDARDS ANALYSIS

<table>
<tr><td colspan="3">Converter performance / durability testing</td></tr>
<tr><td>Standard No.</td><td>Standard title</td><td>Scope</td></tr>
<tr><td>EN 60146-2:2000</td><td>Semiconductor converters - Part 2: Self-commutated semiconductor converters including direct d.c. converters</td><td>This standard applies to all types of semi-conductor converters of the self-commutated type including power converters which contain at least one part of a self-commutated type, for example AC converters, indirect DC converters, direct DC converters.</td></tr>
<tr><td colspan="3">Suitability analysis:
- this standard is a general one, lists parameters that should be measured for converters, but does not describe the measurement methodologies in detail
- this document does not cover durability testing of the power converters
- EMC testing – the methodologies are not consistent with the methods used in the automotive industry
- the standard presents a list of tests that should be performed for converters (p. 7.2; the list can be adapted for LPC testing):
• insulation test
• checking of the protective devices
• light load and functional test (at nominal, minimum and maximum input voltage)
• rated output test
• overcurrent test
• temperature-rise test (at rated load and at the least favorable cooling conditions)
• power loss determination
• measurement of total harmonic distortion (THD) or total harmonic factor (THF)
• measurement of power factor</td></tr>
</table>

- measurement of output voltage (at different loads and input voltages value)
- confirmation of output voltage adjustable range (at rated loads, input voltages)
- output voltage unbalance test (for 3 phase output system)
- Confirmation of output frequency adjustable range
- Output frequency tolerance band test
- Checking of the automatic control
- Short-circuit test.
- Measurement of ripple voltage and current

ISO 21782-1	Electrically propelled road vehicles — Test specification for electric propulsion components Part 1: General test conditions and definitions	This document specifies the test procedures for performance and operating load for voltage class B electric propulsion components (motor, inverter, DC/DC converter) and their combinations (motor system) of electrically propelled road vehicles.

Suitability analysis:

- this standard is general standard: contains terms and definitions and general test conditions for operating points for motor, inverter and motor system, DC/DC converters;

- contains general measurements circuit for inverters and lists required measurements accuracy:

  - Current: ±1,0 %

  -Voltage: ±0,5 %

  - Torque: ±0,2 %

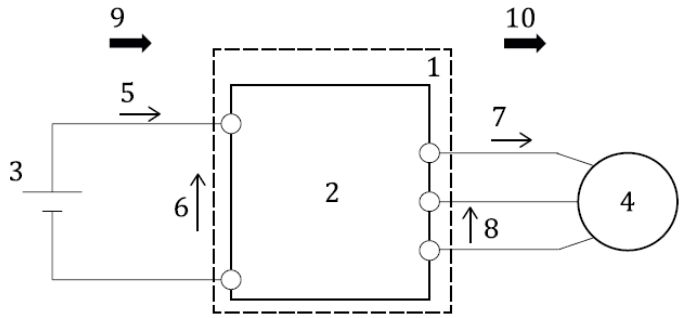
  - Motor speed: ±0,5 %

  - Temperature: ±2 K

  - Relative humidity: ±5 %

  - All measurement values, except temperature and relative humidity values, shall be measured with and recorded at a frequency of not less than 10 Hz.

  For temperature and relative humidity values, a measurement frequency of 1 Hz is sufficient



Key

1	DUT	6	inverter input voltage [V]
2	inverter	7	inverter output current [A]
3	DC power supply	8	inverter output voltage [V]
4	AC load	9	inverter input power [W]
5	inverter input current [A]	10	inverter output power [W]

Current, voltage and power measurement: inverter

ISO 21782-3	Electrically propelled road vehicles — Test specification for electric propulsion components Part 3: Performance testing of the motor and the inverter	This document specifies performance tests for the motor and the inverter designed as a voltage class B electric propulsion system for electrically propelled road vehicles.

Suitability analysis:

+ the standard contains tests applicable **for inverter itself: p. 5.2 Inverter test**

- **5.2.1 Measurement of loss, efficiency and conversion rate** (using the three-wattmeter method is recommended)

- Proposed AC loads: motor, or motor emulator: Electric load which emulates electric characteristic of actual motor, or ACL: 3-phase inductance equivalent to the leakage inductance of the motor; or RL load: ACL with series resistance equivalent to phase resistance of the motor
- Test conditions:

Test conditions	Values	Remark
Inverter input voltage	Rated voltage as defined in ISO 21782-1:2023, 3.23	The DC input voltage shall be in a range of ±2 % of the rated component or system DC input voltage
Operating point	The points as defined in ISO 21782-1:2023, Figure 1 — "a", "b"	In case of no paired motor, a representative current frequency of 200 Hz shall be used. For regenerative operating points, the same operating time applies as for corresponding motoring operating points.
Ambient conditions	Unless otherwise specified, all tests shall be performed at RT of (23 ± 5) °C and with a relative humidity between 25 % to 75 %	

Coolant temperature	Maximum temperature for unlimited operating capability	— In case of liquid cooling — Ethylene glycol and propylene glycol as examples of coolant — If technically feasible, the tests shall be performed at coolant temperature of 65 °C. Otherwise the deviation shall be documented in the test report.
Coolant flow rate	Liquid: Minimum flow rate for unlimited operating capability Air: Value of design specification	
Output frequency	Rated frequency (fr) as defined in ISO 21782-1:2023, 3.21.	
Switching frequency	In accordance with the designed frequency	
Operating time	— The operating point "a": 2 s or 10 s — The operating point "b": 1 800 s	

- Test procedure:
  - The test inverter shall be operated at specified output-current points for the operating time defined in table above. Inverter input power and output power shall be recorded - each average of the last one second of the records shall be used (Annex A of the analysed standard contains information about output power measurement)

  - The efficiency, conversion rate and loss shall be calculated by using formulas:

$$\eta_{i\_conv} = \frac{P_{io\_fund}}{P_{ii\_mean}} \times 100$$

$$\eta_i = \frac{P_{io}}{P_{ii}} \times 100$$

$$P_{il} = P_{ii} - P_{io}$$

ηi	- the efficiency of the inverter including harmonics and ripples (in %)
Pio	- the inverter output power (in W)
Pii	- the inverter input power (in W)
*ηi*_conv	- the conversion rate of the inverter (in %)
*Pio*_fund	- the fundamental inverter output power (in W)
*Pii*_mean	- the average inverter input power (in W)
Pil	- the loss of the inverter (in W)

- **5.2.2 Temperature rise test** (The purpose of this test is to operate the inverter under the specified conditions and to measure the temperature rise in the inverter in order to ensure that the thermal performance of the inverter is as designed)

  - Test conditions:

Test conditions	Values	Remark

Inverter input voltage	Maximum voltage for unlimited operating capability as defined in ISO 21782-1:2023, 3.14.	
Output current	The points as defined in ISO 21782-1:2023, Figure 1 — "a", "b"	
Ambient conditions	Unless otherwise specified, all tests shall be performed at RT of (23 ± 5) °C and with a relative humidity between 25 % to 75 %	
Coolant temperature	Maximum temperature for unlimited operating capability	— In case of liquid cooling — Ethylene glycol and propylene glycol as examples of coolant — If technically feasible, the tests shall be performed at coolant temperature of 65 °C. Otherwise the deviation shall be documented in the test report.
Coolant flow rate	Liquid: Minimum flow rate for unlimited operating capability Air: Minimum flow rate for unlimited operating capability	
Output frequency	Rated frequency (fr) as defined in ISO 21782-1:2023, 3.21.	
Switching frequency	In accordance with the designed frequency	
Operating time	— The operating point "a": 2 s or 10 s — The operating point "b": 1 800 s	

- Test procedure:

  - The inverter shall be operated by the *It*=*t*0, and the temperature of each part of the inverter shall be recorded after the specified time (*t*0) passes.

- The temperature of test inverter shall be measured at the measurement points: electrode part of power semiconductor or specified point of the cooling components closely connected to these parts; inlet and outlet of coolant (additional measurement points can be added).

+ Examples for a test report are given in Annex B.

NOTE: this document does not cover durability testing of the power converters

Standard No.	Standard title	Scope		
ISO 16750 series: ISO 16750-1:2023	 Road vehicles — Environmental conditions and testing for	This document applies to electric and electronic systems and components for vehicles including electric propulsion systems and components. It describes the		

ISO 16750-2:2023 ISO 16750-3:2023 ISO 16750-4:2023	electrical and electronic equipment Part 1: General Road vehicles — Environmental conditions and testing for electrical and electronic equipment Part 2: Electrical loads Road vehicles — Environmental conditions and testing for electrical and electronic equipment Part 3: Mechanical loads Road vehicles — Environmental conditions and testing for electrical and electronic equipment Part 4: Climatic loads	potential environmental stresses and specifies tests and requirements for the specific mounting location on/in the vehicle.
Suitability analysis: - this document does not cover details regarding methodology of functionality check of the DUT and does not include a methodology for measuring basic inverter parameters + this document cover testing of electrical equipment installed inside/on vehicles + ISO 1670 series include the full range of testing: electrical tests, environmental tests, mechanical tests + these standards are the base for most of the OEM standards – a positive test result ensures product acceptance by most end Customers Particular test which applies to the prototyping phase of the LPC are described in p. 5		

Converter safety testing				
Standard No.	Standard title	Scope		
EN IEC 62477-1:2023 (IEC 62477-1:2022)	Safety requirements for power electronic converter systems and equipment – Part 1: General	This part of IEC standard applies to power electronic converter systems (PECA), any specified accessories, and their components for electronic power conversion and electronic power switching, including means for their control, protection, monitoring and measurements. Rated system voltages not exceeding 1000 VAC or 1500VDC		

Suitability analysis:

- this document does not cover: electrical equipment for electric vehicles (according to p. “1 Scope”)

- this document does not cover performance and durability of the power converters

- EMC testing – the methodologies are not consistent with the methods used in the automotive industry

+ analysis of fault conditions and abnormal operating conditions (p. 4.2) can be adapted for LPC converter testing; potential hazards as below:

- Electrically induced mechanical force and thermal hazards (short circuit and overload protection)
- an impact on the decisive voltage determination (but the classification of voltage range should be based on standards for electric vehicles)
- a risk of electric shock due to degradation of protective means
- a risk of energy hazard (visual inspection of the LPC , testing using probes according to ISO 20653 – joined test finger or test rod 2,5mm etc)
- a risk of degradation due to emission of flame, burning particles etc. – protection against fire and thermal hazards
- specific climatic and mechanical conditions (ambient temperature, humidity, vibration, etc.)
- Electrical characteristics (verification of the insulation)
- Micro-environment (pollution)

+ test which can be adapted for LPC testing (according to p. 5.2; after adapting the parameters for use in electric vehicles):

- Protection against foreign objects, dust, water (applies only for LPC with enclosure)
- Impact test (applies only for LPC with enclosure)
- Drop test (applies only for LPC with enclosure)
- Electrical tests (insulation withstand - AC or DC voltage testing)
- Protective equipotential bonding short-circuit ((applies only for LPC with enclosure)
- Output and inputs short-circuit test
- Output overload test
- Cooling failure tests
- Loss of coolant test
- Environmental tests (dry heat, damp heat, dust resistance, vibration tests) – test method based on IEC 60068-2-2; IEC 60068-2-78; IEC 60068-2-6; IEC 60529 – test methodologies consistent with ISO 16750

2.2 CONCLUSIONS

The analysis of the current state of standards regarding inverters was carried out based on publicly available sources of standards such as www.iso.org, www.en-standard.eu, www.cencenelec.eu, www.pkn.pl and using the experience and resources of Bosmal.

A wide range of standards was analyzed in the field of component and system tests, not only for the automotive industry but also for railways and industry; however, particular attention was paid to finding standards dedicated to testing inverters and electrical components.

The analysis shows that there are no standards that comprehensively allow for conducting the inverter testing process. The current scope of standards requires searching for appropriate documents from individual testing fields, and in cases where there is no direct reference to the component, it is necessary to adapt research methodologies, which requires extensive knowledge and experience.

When introducing a specific product to the market, it is known that it is necessary to meet at least the requirements regarding: safety of use, ensuring correct functioning and maintaining the declared parameters in various climatic conditions and under various mechanical and electrical exposures.

The standards system should be supplemented with documents that contain at least a guide/map of documents needed to conduct a comprehensive testing process for a given component. In the next stage, it would be optimal to create standards for the main components of electric vehicles containing a full spectrum of tests (starting from measuring basic characteristic parameters, through checking the functioning under various exposures, to guidelines for carrying out durability tests).

3 LOW-POWER CONVERTER TESTS

Section 3 presents the methods and results of testing the Low Power Converter (LPC) prototypes. The testing methods and measured parameters were selected appropriately for the LPC prototype phase.

The focus was on measuring basic electrical parameters, environmental, durability tests, advanced electrical tests and ensuring safe use, which will be possible to check for subsequent phases of converter development, and for the final High Power Converter (HPC) version, (the scope of possible tests is presented in Section 4).

The UPC converter (Section 3.1) was used for EMI tests, including THD, protections, and efficiencies, while the AIT converter (Section 3.2) was used for efficiencies and system operations at high voltage. Both converters were tested at 800 V DC in the DC bus. The first converter is useful for testing the modulation algorithms and protections that will be implemented in the high-power converter, while the AIT converter is useful for testing the hardware and its test setup.

3.1 UPC LOW-POWER CONVERTER TESTS

The low-power converter developed at UPC is a modular T-type converter, where each phase has its own power and control PCB. The prototype incorporates SiC MOSFETs (SCTH70N120G2V-7) and GaN e-HEMTs (GS66516T). The converter is designed to handle power levels up to 15 kW. A detailed explanation of the design of the converter, including an analysis of the modulation strategies, can be found in D2.1 and D2.3. Figure 3.1 and Figure 3.2 show an image of the power converter.

Figure 3.1: Low-power converter developed by the UPC

Figure 3.2: Low-power converter developed by the UPC

For the tests, on the DC side, a single-phase LISN (Electro-Metrics EM-7820) was supplied by a constant 800-Vdc source. On the AC side, there is an RL load connected in series with R = 68 Ω and L = 1.55 mH.

Voltages and currents were measured with a high-resolution oscilloscope (Agilent InfiniiVision MSO7104A: 1-GHz band-width and 4-GS/s sample rate), and the sensors included in the power converter and detailed in D2.1. For the harmonic distortion calculation, the converter currents were measured with current probes (Keysight N2783B: 100-MHz bandwidth). Moreover, the common-mode voltage was measured using a high voltage differential probe (PMK BumbleBee: 400-MHz bandwidth). These additional voltage and current probes were used because they offer higher bandwidths than the sensors included in the power converter. Therefore, we have used these probes to guarantee accurate results, specially at high frequencies. The converter efficiency was measured using a digital power meter (Yokogawa WT1600: 1-MHz bandwidth).

The modulation techniques were implemented on a dSPACE DS1006 platform and a DS5203 FPGA board. The implemented modulations are the SVPWM and the CB-PWM. Both modulations have been previously examined in D2.3. Figure 3.3 shows a diagram of the experimental setup.

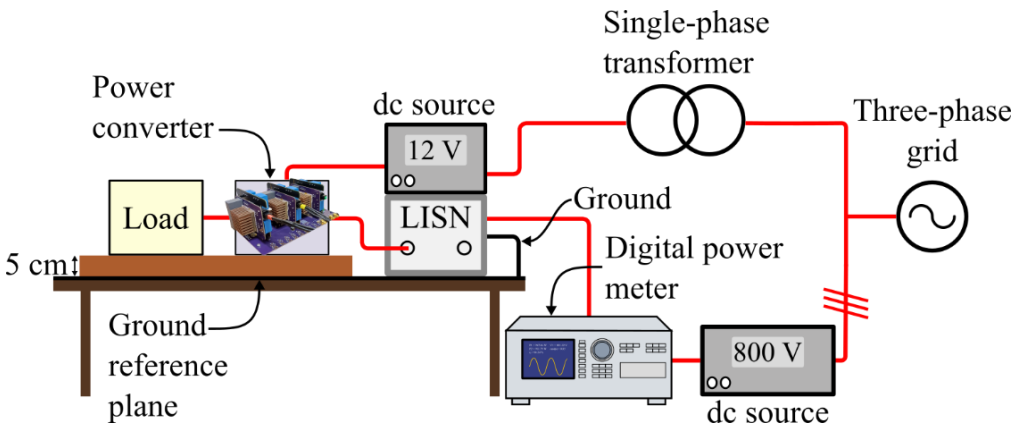


Figure 3.3: Diagram of the experimental setup

3.1.1 EXPERIMENTAL PERFORMANCE

The modulation technique used in the converter plays a critical role in determining power losses, as detailed in D2.3. To evaluate this effect, we compared the efficiencies obtained with the Carrier-Based PWM (CB-PWM) implemented in the power converter against the conventional Modified Sinusoidal PWM (M-SPWM). The study was performed across various output current frequencies to emulate real motor behaviour, as well as at different switching frequencies of 50 kHz and 80 kHz.

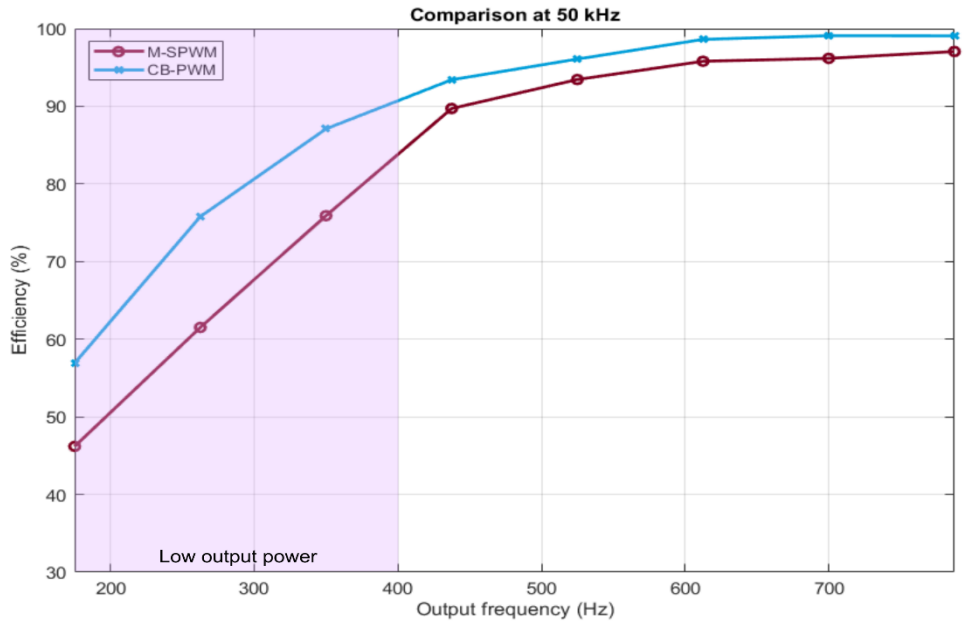
Figure 3.4 illustrates the experimental efficiencies of the T-Type converter under different operating conditions. Before delving into a detailed analysis of the figure, it is important to highlight the two distinct operational zones it represents: the low-output-frequency region, up to approximately 400 Hz, and the high-output-frequency region, beyond 400 Hz. These zones are directly linked to the experimental setup, where the output frequency corresponds to the modulation index, which, in turn, determines the power delivered by the converter.

In the low-frequency region, the converter operates at output powers ranging between 380 W and 1000 W, whereas, in the high-frequency region, the converter delivers higher power levels. At low output power, the currents are relatively small, and the transistors do not operate within their optimal performance region, resulting in low efficiencies. As the output power increases, both voltage and current levels rise, allowing the transistors to operate closer to their nominal specifications. This leads to a characteristic improvement in efficiency as a function of output power, a trend commonly observed across all power transistors.

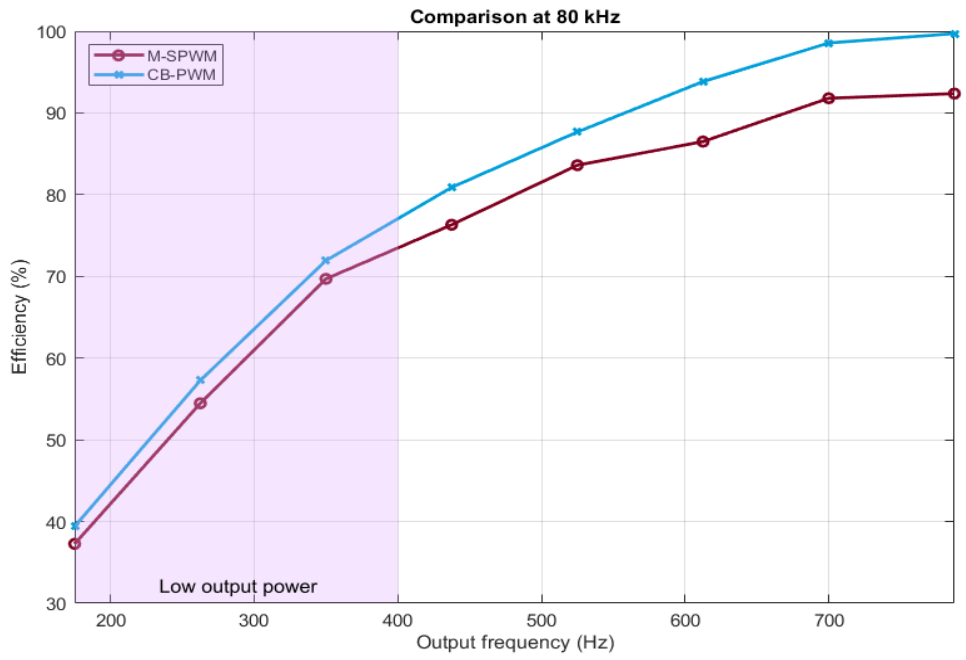
Figure 3.4(a) presents the efficiency results at a switching frequency of 50 kHz. Across all operating points, CB-PWM consistently exhibits higher efficiency compared to M-SPWM, reflecting lower overall power losses. This performance advantage is particularly evident at low output current frequencies, corresponding to low modulation indices. As the output frequency increases, the efficiency gap between the two techniques narrows. At higher output frequencies, CB-PWM achieves efficiencies slightly above 99%, while M-SPWM reaches approximately 97%.

Figure 3.4(b) shows the results at a switching frequency of 80 kHz. Similar to the 50 kHz case, CB-PWM outperforms M-SPWM across all operating points. However, at 80 kHz, the efficiency difference between the two modulation strategies becomes more pronounced at higher output frequencies. This improvement is primarily attributed to the clamping mechanism implemented in the CB-PWM strategy, which selectively locks the semiconductors at specific intervals. This technique not only reduces switching losses but also ensures the balance of the DC bus capacitors.

By minimizing switching losses—particularly significant in SiC-based converters—CB-PWM achieves superior performance. At high output frequencies, CB-PWM maintains efficiencies above 99%, whereas M-SPWM efficiencies drop significantly, reaching approximately 92%.



(a)



(b)

Figure 3.4: Experimental efficiencies at (a) 50 kHz and (b) 80 kHz.

In conclusion, CB-PWM consistently outperforms M-SPWM in reducing power losses, demonstrating superior efficiency across all tested switching frequencies and operating conditions. However, the performance gap between these modulation techniques varies with the operating point, showing the most significant differences at low output and switching frequencies (50 kHz) and high output and switching frequencies (80 kHz). These findings highlight the effectiveness of CB-PWM in optimizing converter performance under a broad spectrum of operating scenarios.

3.1.2 EXPERIMENTAL HARMONIC DISTORTION

To assess the quality of the proposed modulation strategy at low frequencies, the current Total Harmonic Distortion (THD) generated by the CB-PWM technique was compared with that produced by the M-SPWM strategy. The THD measurements consider only the first 40 harmonics, by the IEC 61000-3-2 and IEC 61000-4-7 standards. It is important to highlight that THD is highly dependent on the load connected to the converter. Consequently, the results presented herein should be used solely as a comparative parameter between the studied modulation techniques.

Figure 3.5 illustrates the current THD when the converter operates at a switching frequency of 50 kHz. At this frequency, M-SPWM exhibits a lower THD for nearly all output frequencies. The higher harmonic content of CB-PWM is attributed to the technique's use of transistor clamping at specific moments to minimise switching events and balance the DC bus voltage. As previously noted, this feature improves modulation efficiency but comes at the cost of increased THD. Another notable feature in this figure is the decrease in THD for both modulation strategies as the output frequency increases. However, a peak in THD is observed between 500 and 600 Hz. This occurs because the output frequency is related to the modulation index of the converter. At low frequencies, and thus low modulation indices, the reference vector has a small magnitude, and the converter primarily operates using states 1 and -1, with minimal use of state 0. This continues until the magnitude of the reference vector increases sufficiently to require the use of state 0 with a certain frequency, around m = 0.6. At this point, the converter begins to utilise all three levels, though briefly, which increases THD. As the modulation index rises and the output frequency increases, the converter uses state 0 frequently enough to smooth the output voltage. Consequently, THD begins to decrease, reaching its minimum value around 700 Hz (where the modulation index is 0.8).

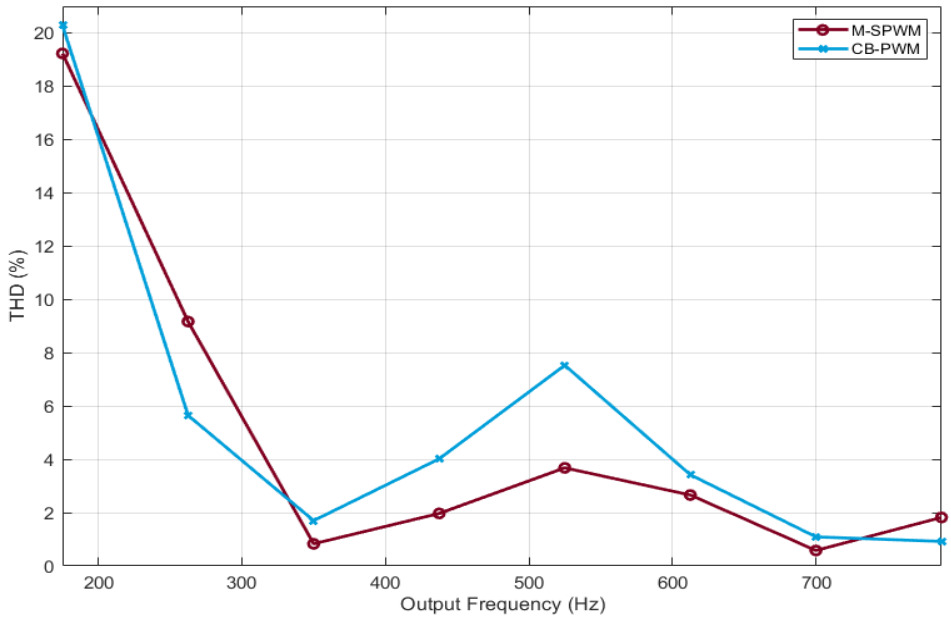


Figure 3.5: Total harmonic distortion generated by the analysed modulation strategies operating at a switching frequency of 50 kHz.

Figure 3.6 shows the current THD when the converter operates at a switching frequency of 80 kHz. In this case, the trend reverses: CB-PWM outperforms M-SPWM in terms of THD, with the latter exhibiting increased harmonic distortion. This behaviour is due to two factors. First, PWM-based modulations generally produce higher harmonic distortion at low frequencies as the switching frequency increases.

Therefore, the THD of M-SPWM is higher at 80 kHz than at 50 kHz. In contrast, the THD of CB-PWM improves at 80 kHz compared to its performance at 50 kHz. This improvement is again attributed to the DC bus balancing algorithm, which samples the DC bus voltages and output currents at each switching instance. With higher switching frequencies, sampling increases, leading to less transistor clamping. While this reduces converter efficiency, it improves harmonic distortion. Moreover, since GaN and SiC semiconductors exhibit low switching losses, the reduction in transistor clamping does not significantly increase losses but does result in a notable improvement in THD.

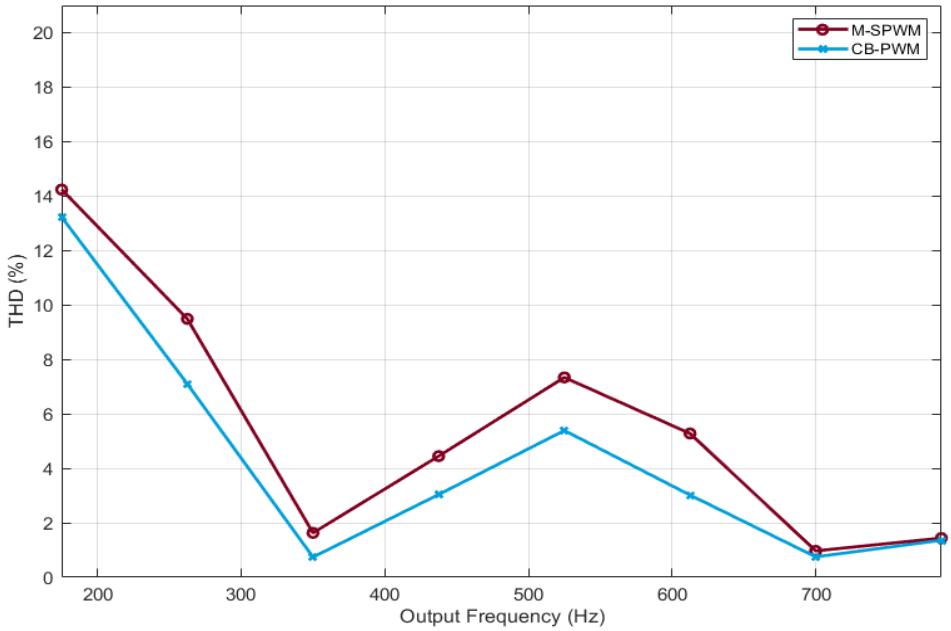


Figure 3.6: Total harmonic distortion generated by the analysed modulation strategies operating at a switching frequency of 80 kHz.

In summary, the results suggest that CB-PWM generally leads to lower harmonic distortion at both switching frequencies compared to M-SPWM. Specifically, at 50 kHz, CB-PWM has slightly higher THD than M-SPWM, but at 80 kHz, CB-PWM demonstrates a significant reduction in harmonic distortion.

3.1.3 EXPERIMENTAL COMMON-MODE VOLTAGE

To analyse the effect of the proposed modulation strategy, we compared the common-mode voltage. All results were obtained at 90% of the maximum output frequency current, which corresponds to modulating a current with a fundamental frequency of 787.5 Hz.

Figure 3.7 shows the common-mode voltage (CMV) generated by the M-SPWM and CB-PWM modulation strategies operating at 50 kHz. For all operating points, CB-PWM produces lower CMV than M-SPWM, both at low and high frequencies. Figure 3.8, on the other hand, presents the CMV when both modulation strategies operate at 80 kHz. In this scenario, CB-PWM still generates lower CMV than M-SPWM. However, the CMVs at 80 kHz are slightly higher than those produced at 50 kHz. This is because CMV is directly dependent on the switching frequency: higher switching frequencies result in higher CMV.

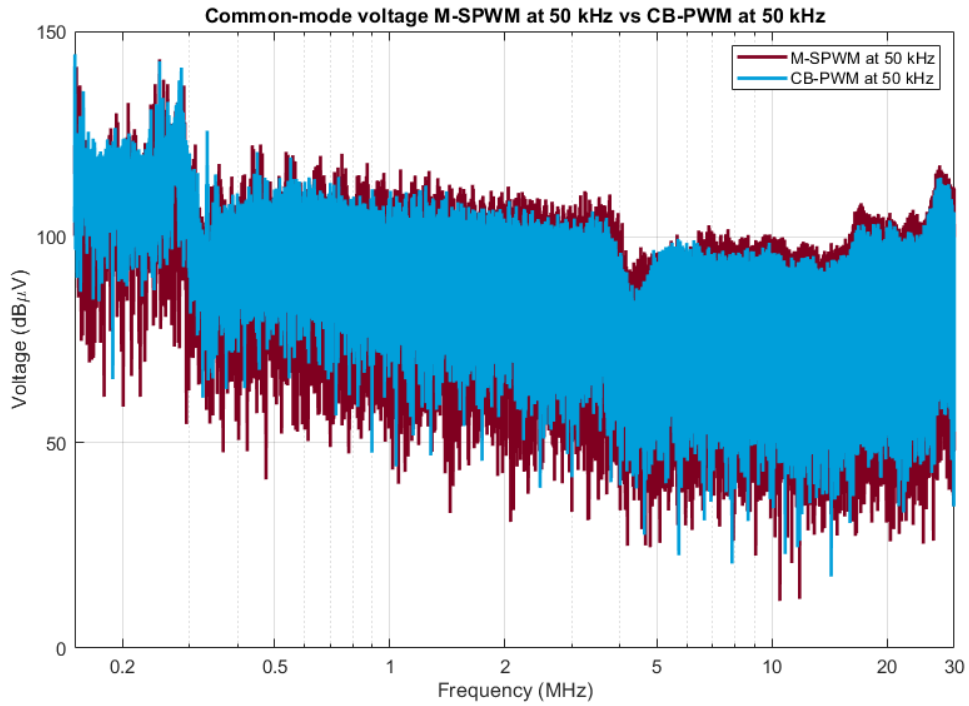


Figure 3.7: Common-mode voltage generated by the analysed modulation strategies operating at a switching frequency of 50 kHz.

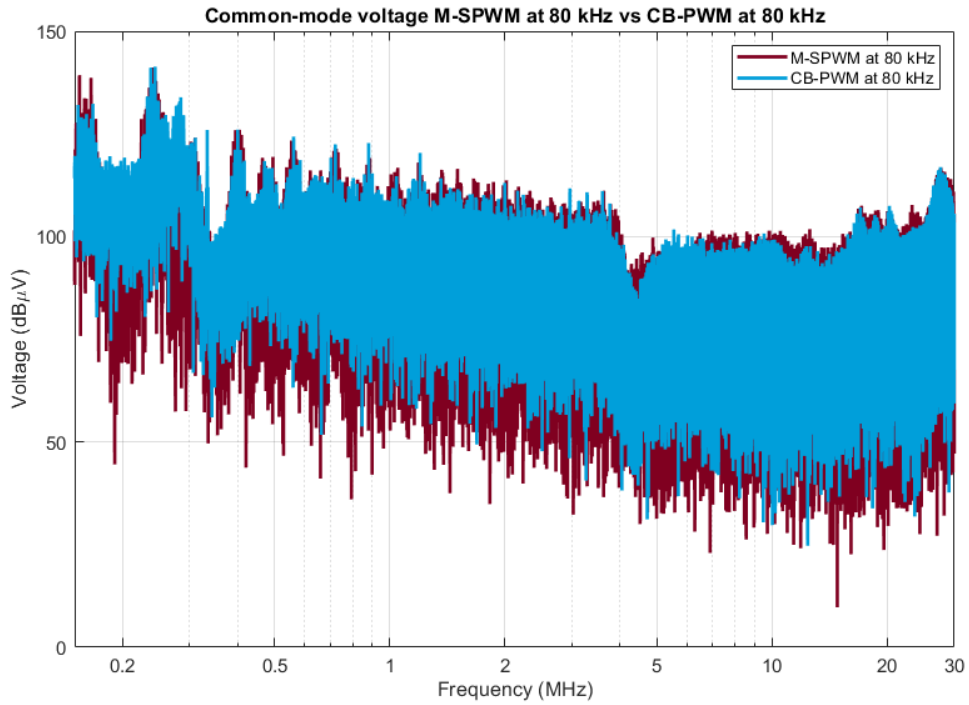


Figure 3.8: Common-mode voltage generated by the analysed modulation strategies operating at a switching frequency of 80 kHz.

This subsection aimed to compare the common-mode voltage generated by two modulation strategies, M-SPWM and CB-PWM, with a focus on their potential applications in high-power converters for electric motors in heavy-duty vehicles.

The results demonstrate that, at both 50 kHz and 80 kHz switching frequencies, CB-PWM consistently produces lower CMV compared to M-SPWM. This reduction in CMV is significant as it directly impacts the longevity and health of the electric motors, making CB-PWM a preferable choice for high-power applications.

3.1.4 EXPERIMENTAL PROTECTION ALGORITHMS

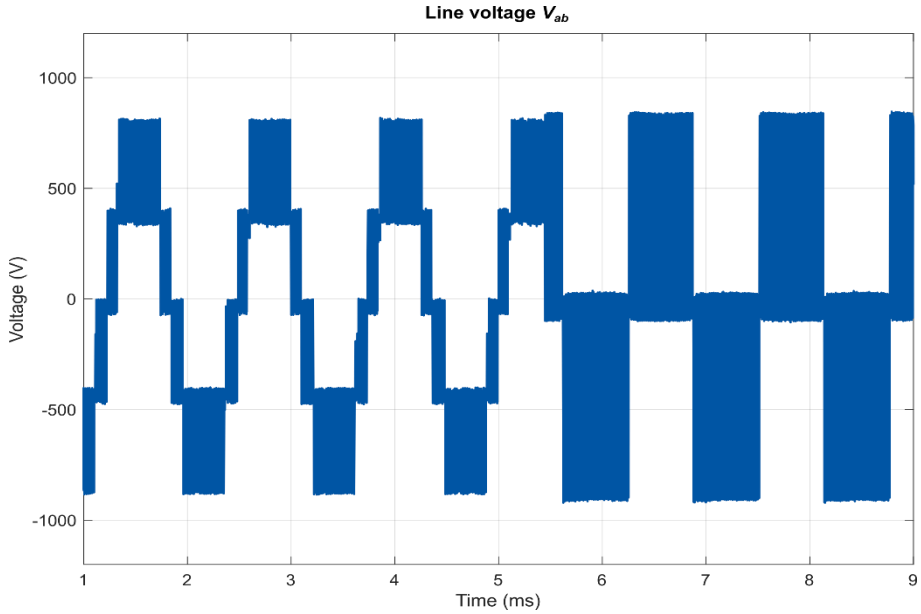
In this experiment, we use the T-Type converter to validate the protection algorithms previously introduced in WP4. Specifically, we test the protection algorithm enabling the converter to transition between three-level and two-level operation. To achieve this, we simulate an overcurrent condition and analyse the converter's response under this condition. Subsequently, the overcurrent alert is removed, allowing the converter to resume three-level operation.

This algorithm was validated with the converter delivering 90% of the maximum output frequency current, corresponding to a fundamental current frequency of 787.5 Hz. The switching frequency was set to 50 kHz. The modulations implemented were CB-PWM for three-level operation and SVPWM for two-level operation.

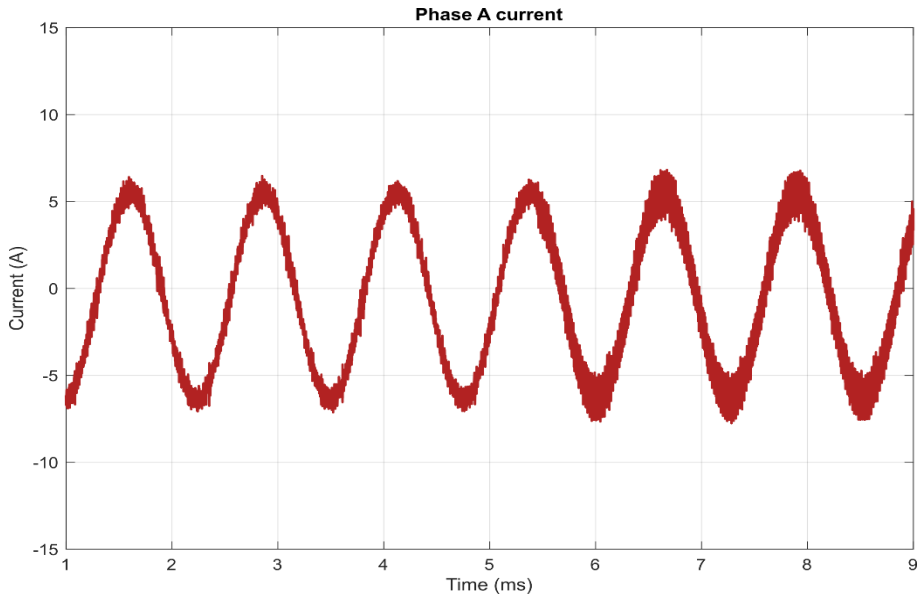
Figure 3.9 illustrates the transition from three-level to two-level operation. This experiment simulates detecting high current levels that GaN transistors cannot withstand. Consequently, these transistors are turned off and remain in that state to prevent current from flowing through them. The converter switches to SVPWM modulation, with only the SiC transistors operating.

Figure 3.9(a) shows the line voltage V_{ab}. Around 5 ms, the overcurrent is detected, and the GaN transistors turn off. This event has a visible effect on the output voltage, which becomes significantly less sinusoidal as only the SiC transistors are switching. Figure 3.9(b) presents the current flowing through phase A.

The impact of the protection algorithm on the system currents is less noticeable, as the currents remain sinusoidal, as expected. However, at the moment of the operational mode change, around 5 ms, the current ripple increases. This effect occurs because the converter now operates with only two voltage levels at the output, resulting in higher harmonic content in the output currents and, consequently, increased ripple.



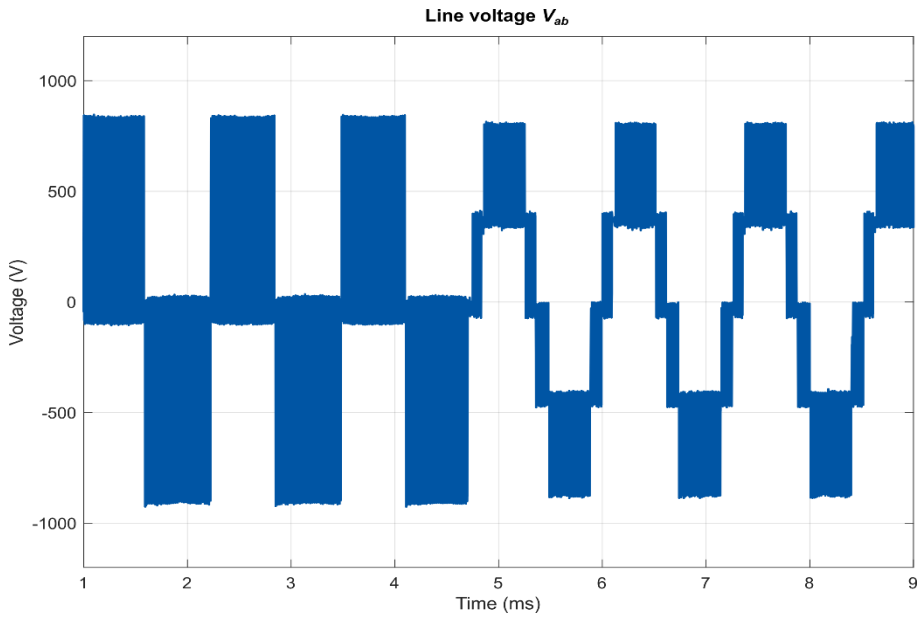
(a)



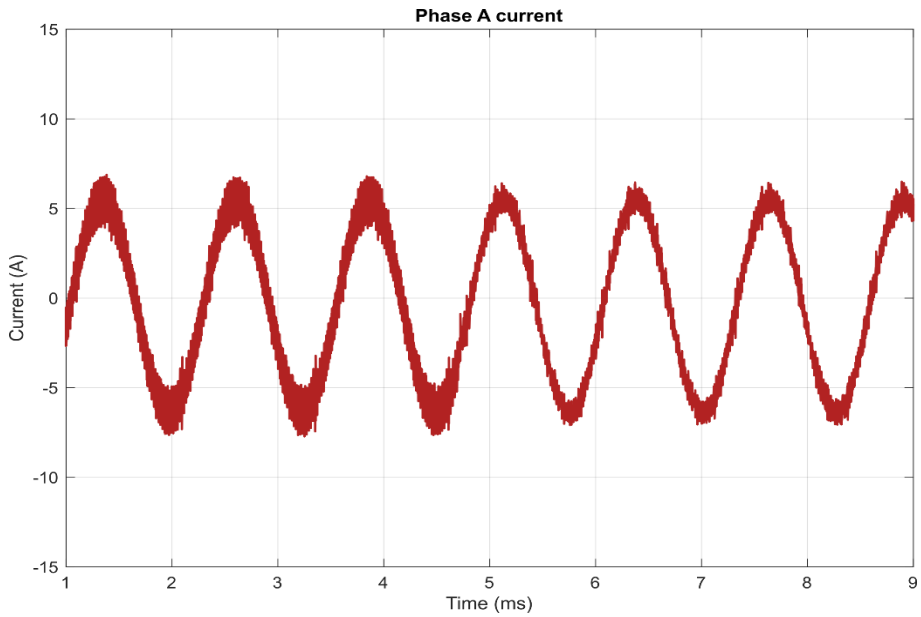
(b)

Figure 3.9: Line voltage Vab (a) and phase A current (b) during the transition from three-level to two-level operation caused by an overcurrent condition.

Figure 3.10 illustrates the complementary operation, transitioning from two-level to three-level operation. This transition occurs when the overcurrent alert is cleared. Consequently, the GaN transistors resume switching, allowing the converter to produce three voltage levels in the phase voltage. Figure 3.10(a) shows the line voltage V_{ab}. Just before 5 ms, the alert disappears, and the converter returns to normal three-level switching. The additional voltage levels resulting from the three-level operation are observed. No voltage spikes occur during the transition from two-level to three-level operation. Figure 3.10(b) shows the current flowing through phase A. The current remains sinusoidal throughout the converter's operation.
However, when the converter operates in two-level mode, the output currents exhibit a greater ripple compared to three-level operation.



(a)



(b)

Figure 3.10: Line voltage Vab (a) and phase A current (b) during the transition from two-level to three-level operation.

The experimental validation demonstrates the effectiveness of the protection algorithms for the T-Type converter, enabling smooth transitions between three-level and two-level operation. During the transition to two-level operation, the converter mitigates excessive current by turning off the GaN transistors and switching exclusively with the SiC devices. This approach prevents potential damage but increases output voltage distortion and current ripple due to the reduced number of voltage levels. When transitioning back to three-level operation, the system resumes normal performance without voltage spikes, restoring smoother output voltages and reducing current ripple.

The results confirm that the protection strategy effectively safeguards the converter under overcurrent conditions while maintaining acceptable performance levels in both

operational modes. Overall, the algorithm ensures system reliability and stable operation under fault scenarios, while minimising adverse effects on output quality.

3.2 AIT LOW-POWER CONVERTER TESTS

A low-power converter has already been conceptualized, simulated, developed and tested at AIT and the details will be presented in the following sections. The details regarding the operation of the converter, as well as the results of simulations and double pulse tests, can be found in Deliverable D2.3

3.2.1 CONVERTER DESCRIPTION AND EXPERIMENTAL SETUP

The AIT low-power converter hardware is shown in Figure . The converter has been built as a modular structure where each of the phases of the power circuit is built on a single PCB, that is identical for all three phases. During assembly, the three PCBs are connected easily to complete the three-phase power circuit with the controller board on top. The filter is also designed on three identical boards, one for each phase.

Such a design helps in quick assembly, debugging, and maintenance. Being modular, the boards can be easily removed and replaced with another module, without disturbing the circuit in other phases.

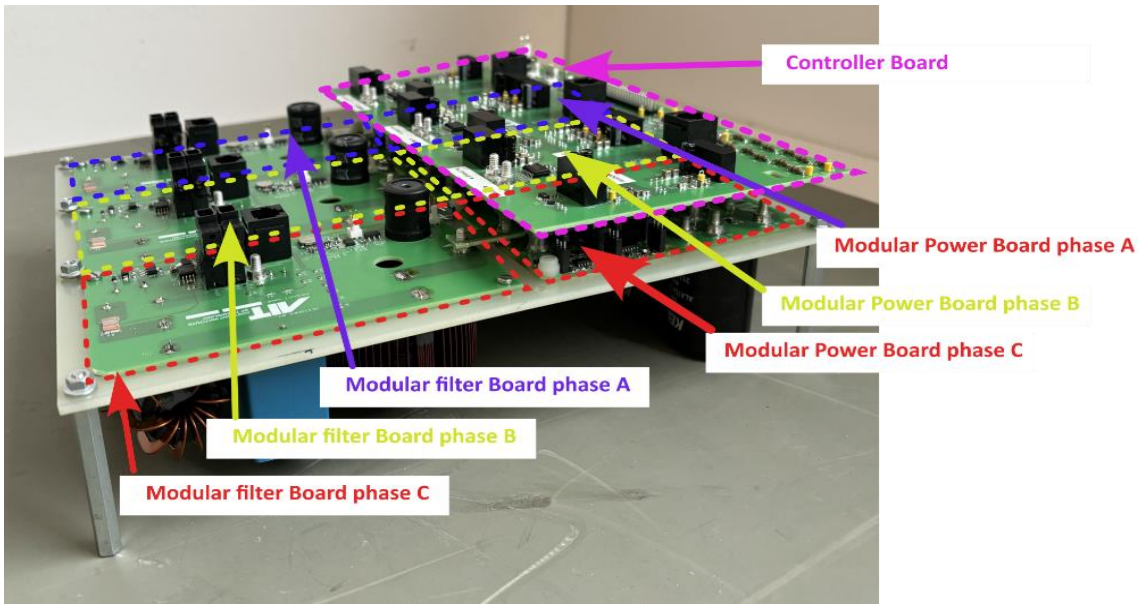


Figure 3.11 Low-Power Hardware for T-Type Converter

For the testing of the low-power converter, two configurations were used.

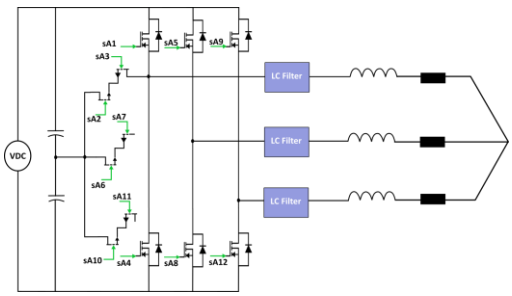


Figure 3.1211 Configuration A for testing the Low-Power converter

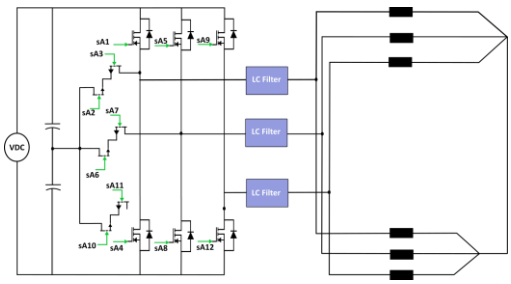


Figure 3.13 Configuration B for testing the Low-Power converter

In the Configuration A, Figure 3.1211 shows the converter connected to a single inductive load. Since the resistive load available in the laboratory was rated for less than 10 kW power, it was connected to two parallel resistive loads in configuration B and this is shown in Figure . The actual test setup is shown in Figure 3.14 and. The controller is implemented in the PLECS RT Box and the PWM signals are provided to the hardware through PLECS Connectors.

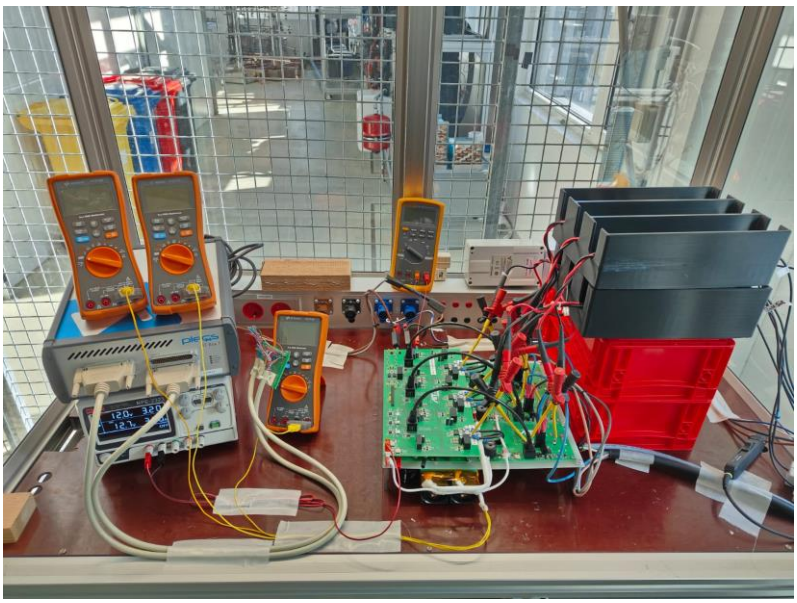


Figure 3.14 Low-power converter test setup

Figure 3.15 Test Setup for Low-power converter with load

3.2.2 EXPERIMENTALS RESULTS

The following figures (Figure and Figure 3.17) shows the experimental results recorded at the oscilloscope seen in Figure 3.15. The waveform in yellow is the DC side current, while the waveform in orange shows the AC side current. The three sinusoidal waveforms in red, green, and cyan show the three-line voltages at the AC side (measured after the filter) and the three pulsed waveforms in red, green, and blue show the AC side output voltage before the filter, measured with respect to the DC midpoint. It can be observed that for the resistive load, the output current is in phase with the AC side voltage, while for the R-L load, the output current is phase-shifted by about 20 degrees.

Figure 3.16 Low-power converter test waveforms at 10 kW resistive load

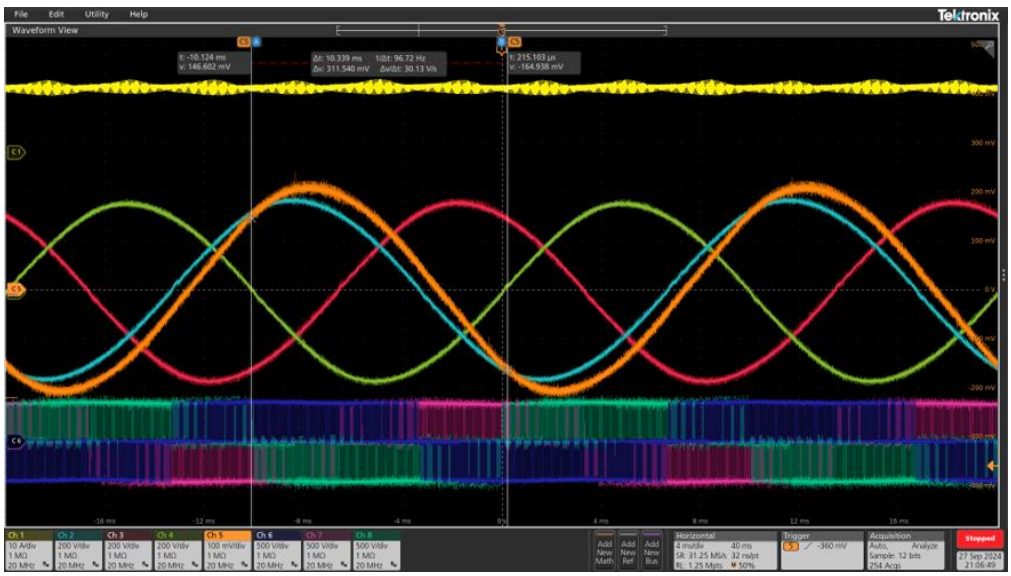


Figure 3.17 Low-power converter test waveforms at 10 kW R-L load

For the Figure , the output power recorded was 10 kW. The AC side load was two 10 Ω resistors connected in parallel. For the Figure 3.17, the output power recorded was also 10 kW but the load connected was 16 Ω resistance, in series with a 10 mH inductor.

The DC bus voltage for both experiments was fixed at 800 V. The inductors were commercially purchased and had a maximum current rating of 15A and this prevented tests at higher power than 10 kW.

For the efficiency calculation, the voltage and current readings at the AC side was recorded at the power analyzer. The DC side power was calculated from the DC supply voltage readings and the DC current was measured using the multimeter.

The graphs in Figure 3.18 to Figure 3.21 show the efficiencies obtained at different voltages. At 200 V, the efficiency recorded was above 99.48 %, at 570 W of output power.

The maximum efficiency recorded at 400V was 99.61 %, at around 2300 W of output power. At 600, the maximum recorded efficiency was 99.54 %, at about 3.8 kW output power. Figure 3.21 shows that the maximum efficiency of the low-power converter was recorded at 99.7 %, for a 7-kW load.

At 10 kW, the recorded efficiency was 99.5 % for a DC voltage of 800 V. All the above efficiencies were recorded for the case of resistive load.

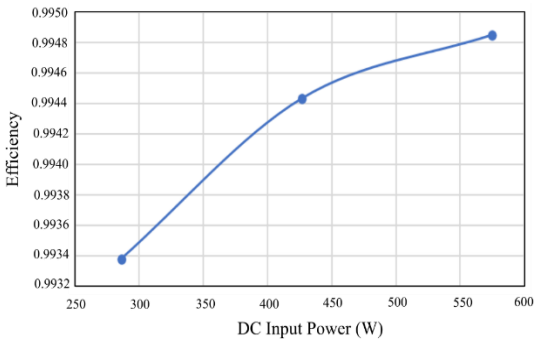


Figure 3.18 Efficiency of the converter at VDC 200V

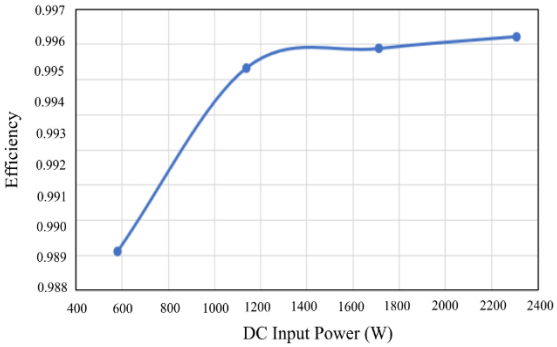


Figure 3.19 Efficiency of the converter at VDC 400V

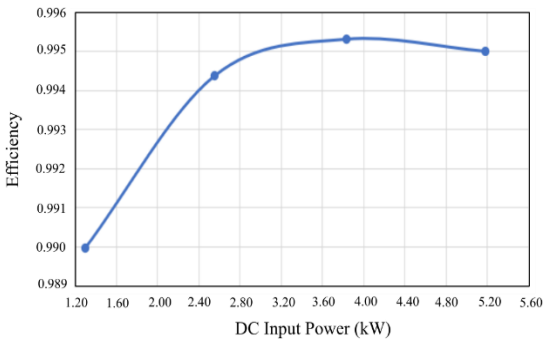


Figure 12 Efficiency of the converter at VDC 600V

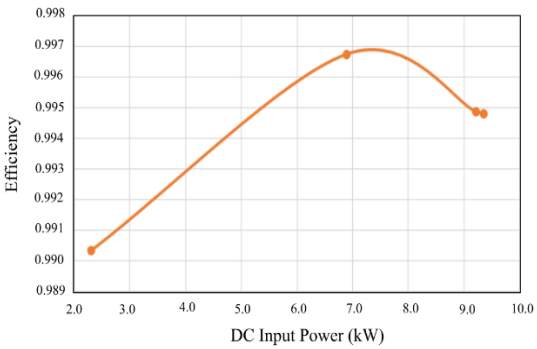


Figure 3.21 Efficiency of the converter at VDC 800V

In the following table, all test data are shown for the test with the R-L load.

Table 3.1 Test Data for RL-Load test for Low-Power Converter

V_{DC} (V)	I_{DC} (A)	P_{DC} (W)	V_{PH1-N} (V)	I_{PH1} (A)	P_{PH1_W} (VA)	P_{PH1_Q} (Var)	V_{PH2-N} (V)	I_{PH2} (A)
804.35	13.354	10741.39	255.07	14.231	3629.90	789.3	256.34	14.11

P_{PH2_W} (VA)	P_{PH2_Q} (Var)	V_{PH3-N} (V)	I_{PH3} (A)	P_{PH3_W} (VA)	P_{PH3_Q} (Var)	P_{AC_TOT} (W)	η (%)
3616.95	776.2	255.03	14.35	3660.95	821.28	10643.48	99.08

The above table shows that 99.08 % efficiency was recorded for the R-L Load case, with a DC bus voltage of 800 V and an output power of 10 kW. It is to be noted that heat sink fan and auxiliary power (negligible at around 25 W) were not included in the efficiency calculations.

3.3 CONCLUSIONS

The experimental investigations of the low-power converters developed by UPC and AIT have provided valuable insights into the performance of hybrid SiC-GaN topologies in power converter systems.

For the UPC low-power converter tests, the effects of Modified Space Vector Pulse Width Modulation (M-SPWM) and Carrier-Based Pulse Width Modulation (CB-PWM) applied to a T-type converter were examined. Experiments conducted at switching frequencies of 50 kHz and 80 kHz assessed efficiency, total harmonic distortion (THD) in the currents, and common-mode voltage (CMV). The results demonstrated that CB-PWM consistently outperforms M-SPWM across all operating conditions:

- **Efficiency**: CB-PWM achieved superior efficiency than M-SPWM, with the performance gap widening at higher switching frequencies.
- **Total Harmonic Distortion**: While M-SPWM exhibited increased THD at higher frequencies, CB-PWM maintained lower THD values, particularly beneficial at 80 kHz.
- **Common-Mode Voltage**: CB-PWM generated lower CMV than M-SPWM, reducing electromagnetic interference—a critical factor in motor drive applications to preserve electric motor health.

The switching frequency plays a crucial role, as it impacts both efficiency and THD results. Higher frequencies slightly reduced efficiencies and affected THD differently for each modulation strategy. Additionally, the protection algorithms implemented were effective, enabling seamless transitions between three-level and two-level operations during fault conditions, thus safeguarding the converter without significant performance loss upon returning to normal operation.

For the AIT low-power converter tests, the focus was on verifying losses and assessing the switching behaviour of circuits combining GaN and SiC semiconductors. Despite the complexity introduced by the hybrid design—necessitating an intricate heatsink—the modular T-type inverter was successfully constructed. Efficiency tests conducted over

15-minute continuous runs recorded efficiencies exceeding 99%, highlighting the substantial performance enhancements achievable with hybrid SiC-GaN topologies.

In summary, both sets of experiments confirm the advantages of using hybrid SiC-GaN converters with CB-PWM modulation strategies:

- **High efficiency:** Achieving efficiencies over 99% demonstrates the potential for energy savings and improved performance.
- **Low THD and CMV:** Reducing harmonic distortion and common-mode voltage enhances the reliability and longevity of connected electric motors.
- **Effective protection mechanisms**: Implementing robust protection algorithms ensures converter safety without compromising operational integrity.

These findings are critical for the RHODaS project as the tested protection algorithms, operating modes, and modulation techniques will be applied to the high-power converter.

4 STANDARDS AND TESTS APPLICABLE TO THE HIGH-POWER CONVERTER

Converters in electric vehicles are integral components of the e-drive system, either integrated within the transmission or as part of the e-axle. This strategic placement ensures that the converters maintain optimal interaction parameters with the electric motor. Given the high switching frequencies of the power modules, it is crucial to keep connections between the converter and the electric motor short to achieve efficient operation.

Testing components for EVs focuses on two primary areas:

- Performance and durability evaluation
- Safety testing

TESTING PROGRAMME PROPOSAL

The initial approach that is being considered for RHODaS prototypes combines a comprehensive testing programme that verifies the converter's resistance to environmental, electrical, and mechanical exposures. This programme is built on international standards and practices employed by vehicle and component manufacturers. The testing programme includes three main areas of testing:

- **Environmental testing:** To assess the converter's performance under various climatic conditions.
- **Mechanical testing:** To evaluate the converter's durability and reliability under physical stress.
- **Electrical testing:** To verify the converter's electrical performance and safety.

Each test proposal includes application evaluations for two scenarios:

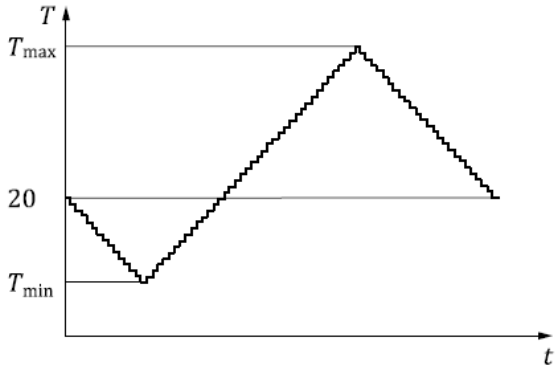
- For the high-power converter installed inside an enclosure with connectors **(C1)**.
- For the high-power converter in its prototype stage, without the enclosure or final connectors **(C2)**.

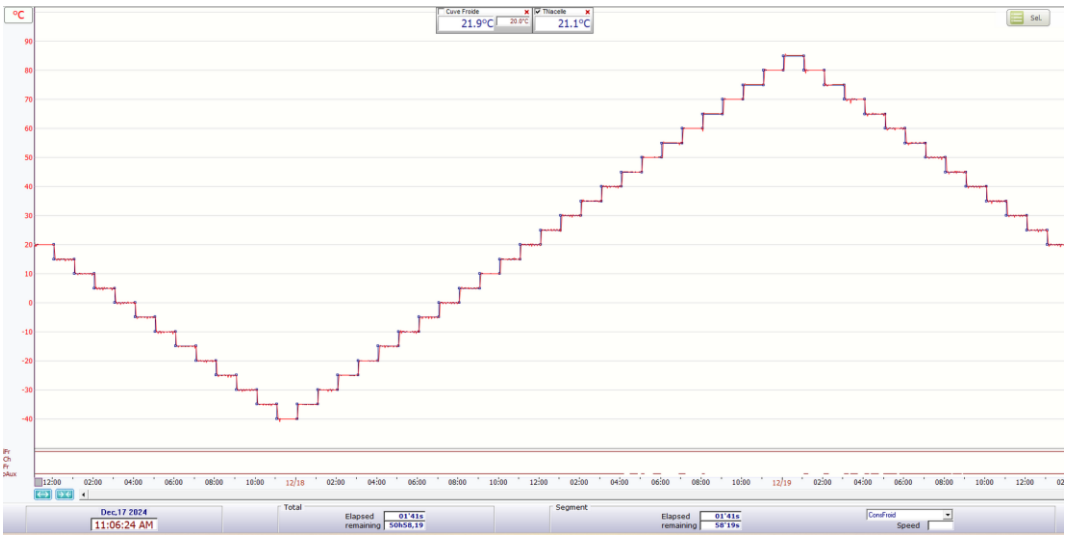
4.1.1 ENVIRONMENTAL TESTING

Tests based on the ISO 16750-4 Road vehicles — Environmental conditions and testing for electrical and electronic equipment — Part 4: Climatic loads and ISO 16750-3:2023 Road vehicles — Environmental conditions and testing for electrical and electronic equipment Part 3: Mechanical loads

1) **(C1) (C2) ISO 16750-4:2023 p.5.2 - Temperature step test** - this test checks the device for malfunctions (including failure to change properly between different operating modes) which may occur within a small section of the operating temperature range.

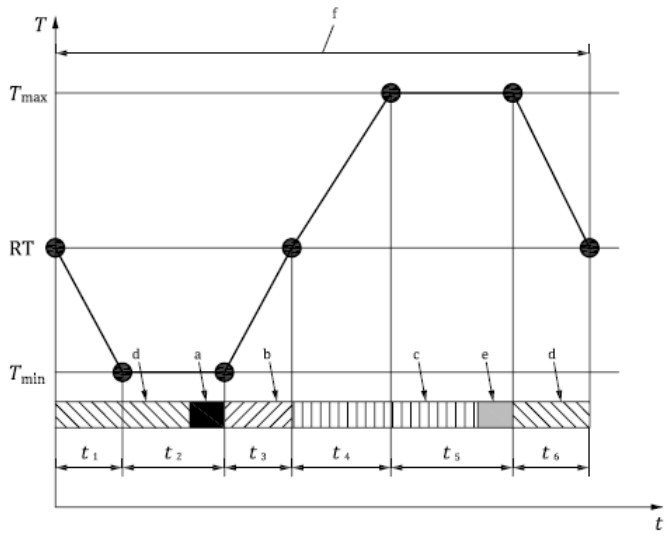
- - decrease the temperature in steps of 5°C from 20 °C to Tmin (-40˚C), then increase the temperature in steps of 5 °C from Tmin to Tmax (+90˚C – for components mounted on the transmission) and then decrease the temperature in steps of 5 °C from Tmax to 20 °C
- Wait at each step for thermal equilibrium + time needed for functional tests (for loaded device and for LV (Low Voltage) / HV (High Voltage)





2) (C1) (C2) ISO 16750-4:2023 p.5.3.1 - Temperature cycle with specified change rate - this test simulates varying temperatures with electrical operation of the LPC, during the use at changing ambient temperature

- the test should be performed with 30 cycles (30x8h=240h); parameters: Tmin = -40°C, Tmax=+90°C, t1=60min, t2=90min, t3+t4=150min, t5=110min, t6=70min, „a" and „e" stage: time needed to perform a functionality check (usually ca. 15min)

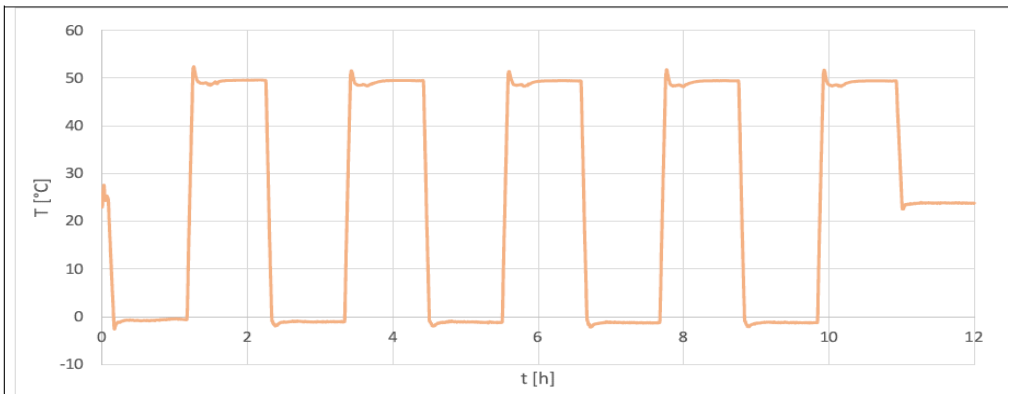


3) (C1) (C2) ISO 16750-4:2023 p.5.3.2 - Rapid change of temperature with specified transition duration - this is an accelerated test which simulates a very high number of slow temperature cycles in the vehicle. The failure mode is an electrical malfunction and/or mechanical failure due to cracking of materials or seal failures caused by ageing and different temperature expansion coefficients

- the test should be performed with 100 cycles (ca 100h); parameters: Tmin = -40°C for 30 min (should be enough for the mass ca 1kg), Tmax=+90°C for 30 min, transfer time < 30 seconds; LPC not powered;

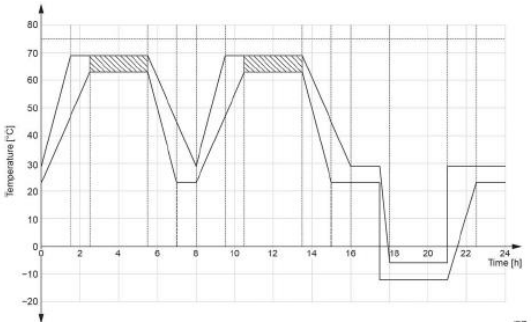
Thermal shock chamber

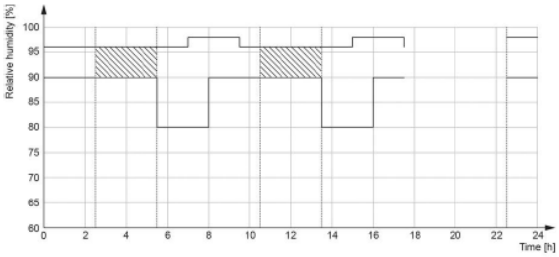
Temperature chart - example



4) (C1) ISO 16750-4:2023 p.5.6.2.3 - Test 2: Composite temperature/humidity cyclic test- this test simulates the use of the LPC under cyclic high ambient humidity. The failure mode is an electrical malfunction caused by leakage current and corrosion. Leakage current and corrosion occurs on a printed circuit board (PCB) or between terminals of external interface connectors due to moisture.; the test in accordance with PN-EN 60068-2-38, Test Z/AD.

- the test should be performed with 10 cycles (10x24h=240h); functional test when the maximum temperature is reached; Tmax 65°C RH 93%; Tmin -10°C





5) (C1) (C2) ISO 16750-4:2023 p.7 - Protection against water and foreign objects - recommended IP class IP6K6K according to ISO 20653:2023

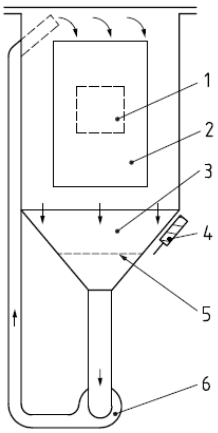
IP6KX – protection against dust ingress

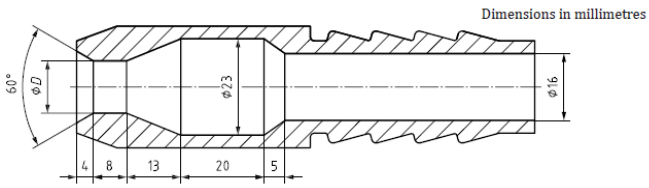
- test dust A2 (Arizona dust) according to ISO 12103-1 shall be used (2 kg of test dust per m3 chamber volume shall be filled in and kept in suspension during the test)

- 6 s movement of the air–dust mixture, 15 min break; 20 such cycles shall be performed.

  IPX6K – protection against water ingress

- Distance 2,5 m to 3 m; 75 l/min ± 5 %; exposure time: min. 3 min





D = 6,3 mm for tests regarding degrees of protection against water 5 and 6K

4.1.2 MECHANICAL TESTING

1) (C1) (C2) ISO 16750-3:2023 p.4.1.7 Test XVII — Commercial vehicle, driving electric motor. This test checks also components attached to the electric motor, such as an inverter for malfunctions and/or breakage caused by vibration.

Random vibration; The test duration is 32 h for each axis of the LPC; The RMS acceleration values for three primary axes:

- X and Y: 26,8 m/s2,
- Z: 37,2 m/s2.

Table 4.1: PSD profile. Temperature profile superimposed on vibration profile

X and Y axis		Z axis	
Frequency [Hz]	**PSD [(m/s²)²/Hz]**	**Frequency [Hz]**	**PSD [(m/s²)²/Hz]**
10	9	10	20
35	9	30	20
100	0,2	90	0,4
2 000	0,2	2 000	0,4

Parameter	Duration [min]	Temperature [°C]
t_1	60	From RT to T_{min}
t_2	90	Exposure time at T_{min}
t_3	60	From T_{min} to RT
t_4	90	From RT to T_{max}
t_5	110	Exposure time at T_{max}
t_6	70	From T_{max} to RT
NOTE T_{min} and T_{max} are defined in ISO 16750-4:2023, Table 1.		

Tmin = -40°C, Tmax=+90°C

At the end of the cold and hot phase functionality check is performed (LPC powered and loaded).

Note 1: The LPC should be mounted to a vibration jig with appropriate characteristics (the resonance frequencies of the vibration jig will affect the test result).

Note 2: The DC/AC inverter is targeted for TRL6, meaning that the equipment's functionalities must be demonstrated in a realistic operating environment, where it is possible to draw conclusions about the technical and operational capabilities of the product.

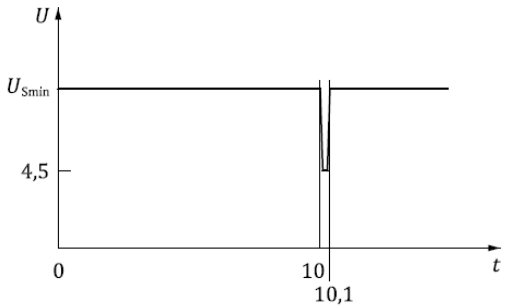
Some features of a more advanced industrial design (TRL7/TRL8) might not be available in this beta version of the DC/AC converter, such as features linked to the final design, such as mechanical or EMC features.

4.1.3 ELECTRICAL TESTING

Electrical testing – testing of the LV part, according to ISO 16750-2:2023 Road vehicles — Environmental conditions and testing for electrical and electronic equipment Part 2: Electrical loads.

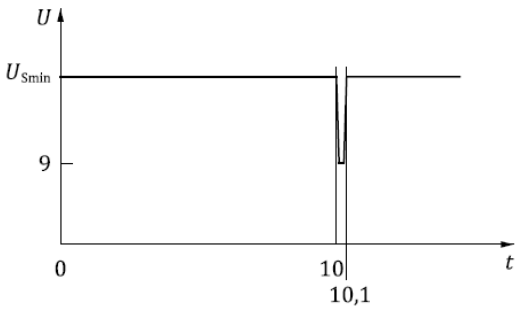
1) (C1) (C2) ISO 16750-2:2023 p.4.6.1.1 Momentary drop in supply voltage – this test simulates the effect when a conventional fuse element melts in parallel circuit.

Apply the test pulse simultaneously to all LV supply lines and check the behavior of the LPC.



Key

t	time, in seconds
U	test voltage, in volts
U_{Smin}	minimum supply voltage, in volts



Key

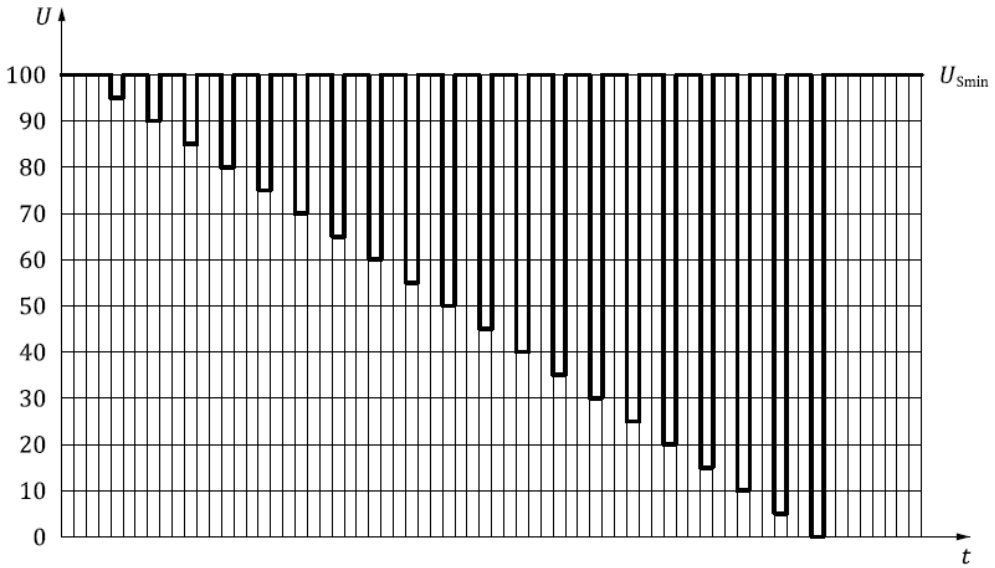
t	time, in seconds
U	test voltage, in volts
U_{Smin}	minimum supply voltage, in volts

Us for 12V system: Usmin = 10.5V Usmax = 16V

Us for 24V system: Usmin = 18V Usmax = 32V

2) (C1) (C2) ISO 16750-2:2023 p.4.6.2 Reset behaviour at voltage drop – this test verifies the reset behaviour of the LPC at different voltage drops

Apply the test pulse simultaneously to all LV supply lines and check the reset behaviour of the LPC



Key

t	time, in seconds
U	test voltage measured as a percentage of U_{Smin}
U_{Smin}	minimum supply voltage, in volts

Us for 12V system: Usmin = 10.5V Usmax = 16V

Us for 24V system: Usmin = 18V Usmax = 32V

3) (C1) (C2) ISO 16750-2:2023 p. 4.9.1 Single line interruption – this test simulates an open contact condition, for instance, if a single wire or electrical connection to a HPC has an interruption. This test is applicable for both power, ground, signal and load circuits for the LPC.

Connect and operate the LPC as intended. Open one circuit of the HPC, then restore the connection. Observe the device behaviour during and after the interruption.

Perform this test for load-circuits in addition with the conditions for:
- outputs active;
- outputs inactive.

Repeat for each circuit of the HPC. The following test conditions shall be met:
- interruption time: (10 ± 1) s;
- open circuit resistance: ≥ 10 MΩ;
- maximum interrupt transition time ≤ 10 ms.

4) (C1) (C2) ISO 16750-2:2023 p. 4.9.2 Multiple line interrupt – The purpose of this test to ensure appropriate functional status when the HPC is subjected to a rapid multiple line interruption, for instance if the whole connector to the HPC is unplugged.

Disconnect the LPC connector, then restore the connection. Observe the device behavior during and after the interruption.

The test shall be run once with the HPC powered but without the load, and once with the HPC loaded.

The following test conditions shall be met:

- interruption time: (10 ± 1) s;

- open circuit resistance: ≥ 10 MΩ.

For multi-connector devices, each possible connection shall be tested.

5) (C1) (C2) ISO 16750-2:2023 p. 4.10 Short circuit in signal lines and load circuits and overload protection – These tests simulate short circuits and overload to the inputs and outputs of a device.

Short circuit

Connect all inputs and outputs (both signal lines and load circuits) of the HPC in sequence for duration of 60 s ± 10 % to USmax and to ground, as described below in steps a) through f). All other inputs and outputs remain open.

a) Connect DUT signal line/load circuit to be tested to USmax.

b) Hold short circuit condition for a duration of 60 s ± 10 %.

c) Observe behaviour of DUT during and after holding time in b).

d) Connect DUT signal line/load circuit to be tested to ground.

e) Hold short circuit condition for a duration of 60 s ± 10 %.

f) Observe behaviour of DUT during and after holding time in e).

Repeat steps a) through f) for all signal lines and load circuit inputs/outputs of the DUT.

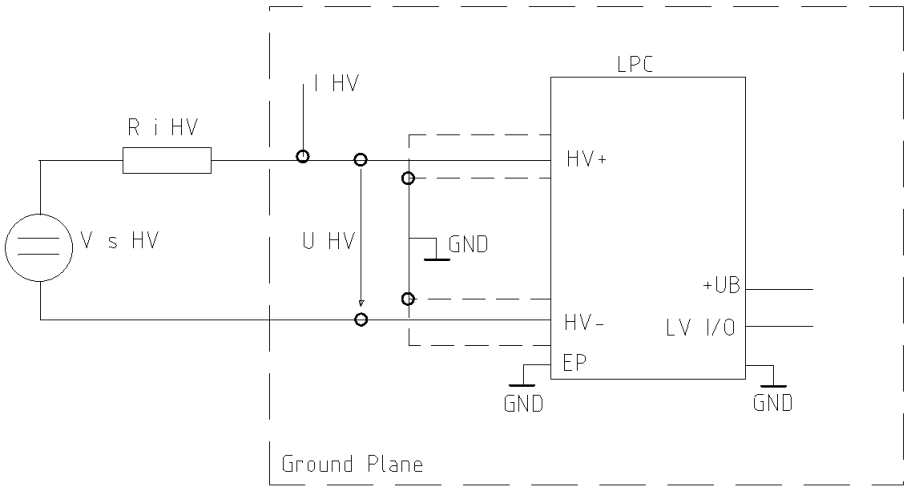
Complete test set as described above shall be performed one time for each of the conditions given below:

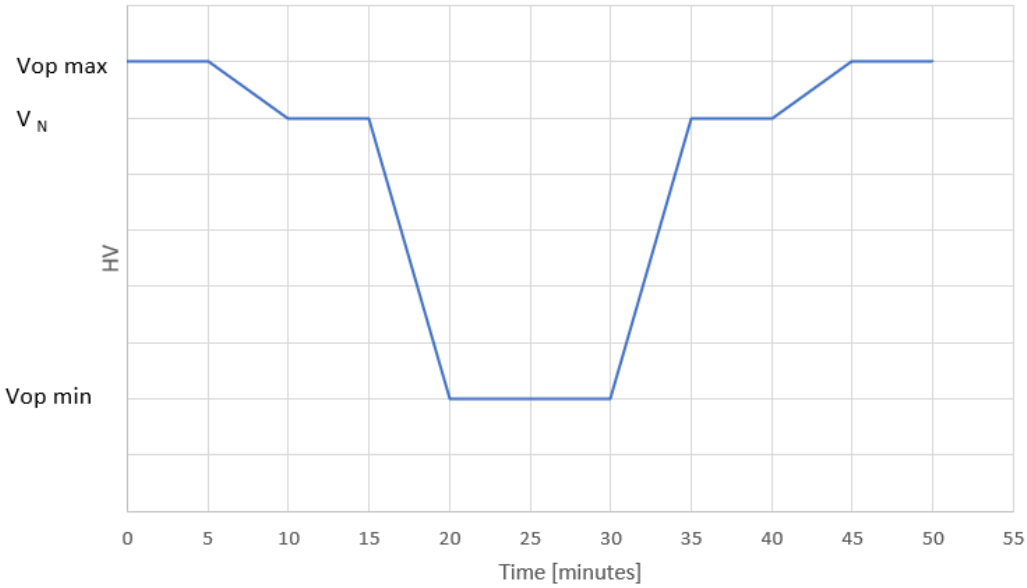
- connected supply voltage and ground terminals:
    - outputs active;
    - outputs inactive;
- disconnected positive supply voltage terminals (this addresses effects of inverse current by, for example, removal of the HPC cable harness fuse, while short to positive supply is present on signal lines and load circuit).

- **Electrical testing – testing of the HV part; based on the OEM standards:**

1) (C1) (C2) HV voltage curve in the regular HV operating voltage range

Setup:

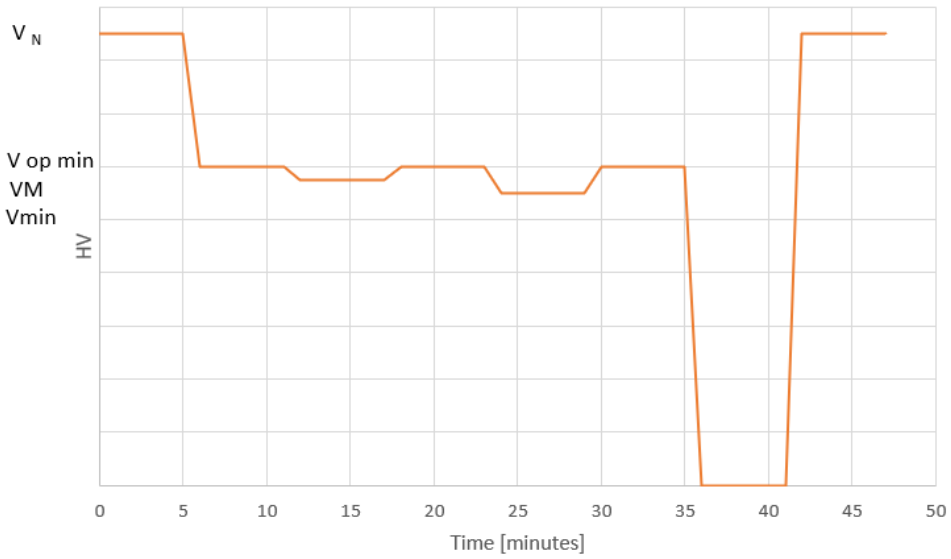


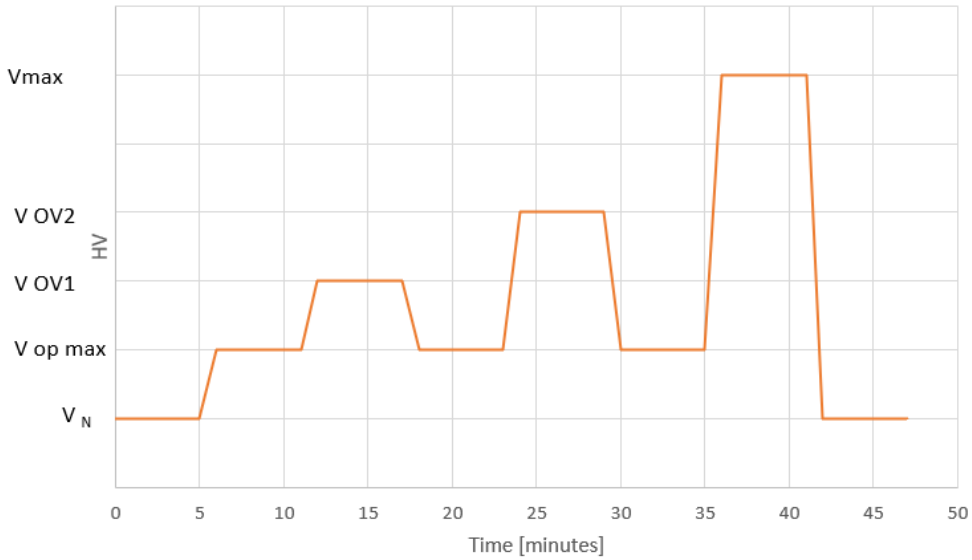


Vs HV - HV voltage source
Vop max - operational voltage max - should be defined
V_N - operational voltage nominal
Vop min - operational voltage min - should be defined
Ri HV – ohmic internal resistance = 0 ohm
I HV – current probe
U HV – HV probe
EP – equipotential bonding connection
Temperatures: Tmin, Tmax, T_{RT}

2) (C1) (C2) Operation within the HV overvoltage range / undervoltage range

Electrical setup as in p. 1



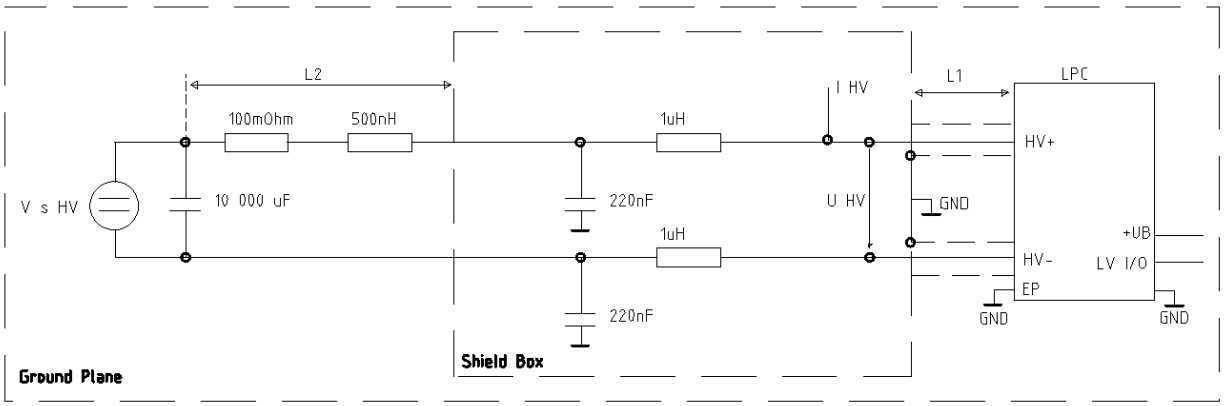


Vop max - operational voltage max - should be defined
Vop min - operational voltage min - should be defined
V_N - operational voltage nominal
V max - voltage max - after exceeding this value, HPC switches off
V min - voltage min - after exceeding this value, HPC switches off
VM = Vop min – (Vop min – Vmin) / 2
V OV1 – below the overvoltage detection
V OV2 - above the overvoltage detection and below the shutdown threshold
Temperatures: Tmin, Tmax, T_{RT}

- **Electrical testing – testing of the HV part:**

3) (C1) (C2) Generated HV voltage ripple

Setup:



The ripple contents superimposed on the DC HV supply voltage and the DC HV supply current must be tested.

Spectrum analyzer, data logger, or oscilloscope with a fast Fourier transform (FFT) function is needed.

Temperatures: Tmin, Tmax, T_{RT}

Requirements:

Measuring frequency range f 10 Hz to 150 kHz

Maximum voltage ripple up to and including the constant power output : 900 V DC vehicle electrical system: 16 Vpp

Short-term, maximum voltage ripple in the time domain above the constant power output (static and dynamic): 900 V DC vehicle electrical system: 32 Vpp

In the frequency domain:

900 V DC vehicle electrical system:

10 Hz to 2 kHz 12 Vpp

2 kHz to 5 kHz 12 Vpp to 19 Vpp (frequency log scale)

5 kHz to 40 kHz 19 Vpp

40 kHz to 50 kHz 19 Vpp to 6 Vpp (frequency log scale)

> 50 kHz 6 Vpp

5 CONCLUSIONS

A comprehensive review of the existing standards was conducted to assess their applicability to the new generation of power converters developed in the RHODaS project.

A series of measurements were performed to evaluate the hybrid T-type inverter topology. The findings from the low-power inverter tests indicate that efficiency can be significantly improved using the proposed hybrid SiC-GaN T-type topology.

This deliverable also examines the effects of advanced modulation techniques such as Modified Space Vector Pulse Width Modulation (M-SPWM) and Carrier-Based Pulse Width Modulation (CB-PWM) on the T-type converter within the RHODaS project.

Efficiency, total harmonic distortion (THD), and common-mode voltage (CMV) were evaluated at switching frequencies of 50 kHz and 80 kHz, high voltages (800 VDC) and medium power (5 – 10 kW).

The experimental results demonstrate that CB-PWM achieves higher efficiency and lower CMV under all conditions and frequencies. Although M-SPWM shows lower THD at lower frequencies, its THD increases significantly at higher switching frequencies. In contrast, CB-PWM maintains lower THD at higher frequencies, making it the preferred modulation strategy for such conditions. Additionally, CB-PWM generates fewer electromagnetic interferences, which is critical for motor drive applications.

The effectiveness of the protection algorithms was also validated, ensuring seamless transitions between three-level and two-level operations and safeguarding the system. This confirms that CB-PWM is the optimal modulation strategy due to its superior efficiency and CMV reduction.

Low-power converters were tested at 800 V, while the high-power converter will operate at voltages between 1000 and 1200 V. However, the obtained results can be directly transferred to the high-power converter. The comparison between modulations is independent of the DC bus voltage. Hence, CB-PWM modulation, which will be applied in the high-power converter, will consistently outperform M-SPWM in terms of THD, CMV, and efficiency. However, the bus voltage will influence the exact values of these parameters. Additionally, the protections and operating modes of the power converter are also independent of the bus voltage, making them fully applicable to the high-power converter.

Some of the developed techniques will be applied to the high power converter (150kW), which will be tested under the applicable standards according to the descriptions in this document to validate its benefits. Moreover, the analysis of research methodologies revealed a significant gap in the standards for the comprehensive testing of power converters, particularly for automotive applications. The current standards require an in-depth analysis of numerous documents to create a comprehensive test plan. This plan must ensure the correct, efficient, and safe operation of the power converters over their intended operating period.

Overall, this deliverable has allowed for a thorough analysis of existing standards, the proposal of a test plan, and the verification on a real prototype of the modulation algorithms developed in WP2 and the protection mechanisms from WP4.

Regarding the deviations of the deliverable, it has been delayed a few months from the scheduled date. The main reason for the delay was the development and manufacturing of the converter heatsinks. These heatsinks were custom-designed to adapt to the height difference between the thermal plane of the PCB and the GaN. Additionally, their design considered the need to quickly dissipate the heat from the GaN transistors due to their

low thermal conductivity and small size. The delay in manufacturing these heatsinks postponed the start of testing with the low-power converters and, consequently, the deliverable. However, this delay did not affect the rest of the project, as the deliverable results, especially the new modulations and protections for the high-power converter, were completed before the high-power converter had been fully tested, i.e., before finishing D5.1 and D5.2. Consequently, the transfer of the deliverable results has been completed within the originally planned timeframe.

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ISO 16750-3:2023 Road vehicles — Environmental conditions and testing for electrical and electronic equipment Part 3: Mechanical loads

ISO 16750-4 Road vehicles — Environmental conditions and testing for electrical and electronic equipment — Part 4: Climatic loads

VW 80300: 2021-02 - Electrical and electronic high-voltage components in motor vehicles

ISO 21782-1 Electrically propelled road vehicles — Test specification for electric propulsion components — Part 1: General test conditions and definitions

ISO 21782-3 - Electrically propelled road vehicles — Test specification for electric propulsion components — Part 3: Performance testing of the motor and the inverter

EN IEC 62477-1:2023 - Safety requirements for power electronic converter systems and equipment – Part 1: General

EN 60146-2:2000 - Semiconductor converters - Part 2: Self-commutated semiconductor converters including direct d.c. converters

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