D2.2. Active gate drivers for high-power, high-frequency WBG devices

Reinventing High-performance pOwer converters for heavy-Duty electric trAnSport

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DISCLAIMER

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AGD	Active gate drivers
ASIC	Application-specific integrated circuit
CPLD	Complex programmable logic device
DESAT	Desaturation
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FPGA	Field programmable gate array
GD	Gate driver
GDC	Gate driver circuit
GaN	Gallium nitride
IC	Integrated circuit
LUT	Lookup table
OC	Over current
OVLO	Over-voltage lockout
PLL	Phase-locked loop
MCU	Microcontroller unit
MMCM	Mixed-mode clock manager
SiC	Silicon Carbide
UVLO	Under-voltage lockout
WBG	Wide bandgap

EXECUTIVE SUMMARY

Active gate driving has been shown to provide reduced circuit losses and improved switching waveform quality in power electronic circuits. Featuring higher switching speed and lower losses, the silicon carbide MOSFETs and GaN devices are widely used in higher power density and higher efficiency power electronic applications as a new solution. However, the increase of the switching speed induces oscillations, overshoots, electromagnetic interference (EMI) and even additional losses.

High – voltage, high – power T-Type RHODaS SiC/GaN inverter uses power devices working at 1000VDC in DC bus, while intermediate GaN leg has to support 500VDC as a rated voltage. Reducing voltage and current overshoots becomes crucial to allow the use of 650V GaN, which represent the current available technology.

This deliverable studies, develops and tests a novel active gate driver (AGD) for high-power GaN switches, that allows to fully using its potential of high-speed characteristic under different operation temperatures and load currents. The principle of the AGD is based on drive voltage decrement during the voltage and current slopes since high dV/dt and dI/dt are the source of the overshoots, oscillations and EMI problems. This voltage control is achieved by a duty-adjustable high frequency pulse train generated by a FPGA that modifies the input and output sides of the PWM pulses applied to the gate of the transistor, thus generating a variable drive voltage that change according the switching conditions. Compared to conventional gate driver (CGD) with fixed drive voltage, the proposed AGD has the capability of suppressing the overshoots, oscillations and reducing losses without compromising the EMI.

Analytical developments, simulations and experimental results are showed in the deliverable, which are the basis for the future utilization of these advanced gated drivers in RHODaS power converters.

1. INTRODUCTION

1.1 DESCRIPTION OF THE DOCUMENT AND PURSUE

Gate driving methods for GaN transistors based on gate current control, gate resistance change, or gate-source voltage (V_{gs}) modifications are essential issues for improving GaN devices, enhancing existing GD circuits, and allowing advanced new GD systems, especially for high-voltage and high-power applications.

Therefore, this deliverable presents the analysis and development of advanced gate drivers for SiC MOSFETs and GaN devices, which could be used as Active Gate Drivers (AGD) in commercial power converters. The document also describes the usual, commercial gate drivers, their functions, advantages, and disadvantages. In addition, the issues and challenges of using commercial gate drivers (GDC) and encounters when designing with new gate driver circuit approaches are discussed, particularly for GaN transistors.

The document includes a gate-driving approach for GaN power devices and the proposal's modelling, design, and parameter definitions. The gate-driving is fully evaluated using LTspice for simulations and validated with laboratory tests. Finally, an AGD based on gate driving is delineated to be applied to WBG semiconductors like those used in RHODAS converters.

1.2 WPS AND TASKS RELATED WITH THE DELIVERABLE

This deliverable refers to Task 2.3 included in WP2: Design of electric and electronics components.

2. GATE DRIVERS OVERVIEW

2.1 GATE DRIVERS' ISSUES AND REQUIREMENTS

Wide Bandgap (WBG) devices, such as silicon carbide (SiC) and Gallium-Nitride (GaN) transistors, are expected to address new power converter requirements. Their improvements in intrinsic characteristics concerning high-speed operation, high voltages, current processing, and low power dissipation allow them to achieve high efficiency and high-power density converters [1], [2]. Compared to SiC MOSFETs, GaN transistors can operate at higher speed with lower on-state resistance ($R_{DS,ON}$), leading to low switching losses and enabling high-efficiency power converters [3], [4]. Nevertheless, high-speed operation of the GaN transistor causes ringing and overshoots in the voltages and currents, which can induce electromagnetic interference (EMI) and even destroy the transistors [5], [6]. Therefore, high switching frequency requires more attention on circuit designs to reduce parasitic elements significantly.

Gate drivers (GD) are fundamental components that ensure the operation of power transistors. There are many GD solutions for switching power devices, which integrate simple functions and advanced functionalities. In deliverable D2.1 were presented some commercial GD integrated circuits (IC) and their main characteristics were introduced, which can be summarized as follows:

- **Voltage and Current Control:** Gate drivers supply the voltage and current required to turn a power semiconductor device on or off. They guarantee that sufficient energy is applied to the gate for effective switching.
- **Speed of Operation:** Gate drivers should be able to turn power devices on and off quickly. Power electronic systems must transition quickly to reduce power losses and increase efficiency.
- **Enable and disable function:** Certain applications demand independent control of the driver's output state without involving the input signal. Some GDs have a pin offering an enable and disable function to achieve this requirement.
- **Isolation feature**: It is the electrical separation between various functional circuits in a system, so no direct conduction path is available between them. This allows individual circuits to possess different ground potentials. Signals can still pass between isolated circuits using inductive, capacitive, or optical methods. For a system with gate drivers, isolation may be a safety requirement and also necessary for functional purposes. For example, in power converter topologies such as half-bridge and full-bridge, the upper power devices require an isolated gate driver because the source is not connected at the ground potential (floating).
- **Driving high-power devices:** Significant gate driving currents are needed to switch power devices efficiently in high-power applications. Then, GDs should be made to support and drive such high currents and guarantee the reliable operation of power devices.
- **Dead time feature:** Ensuring minimal dead time between the high−side and low−side gate drive output signals is critical for the safe, reliable, optimized operation of any high−speed, half−bridge power stage.
- **Monitoring and communications interface:** The new generation of GDs includes features for monitoring GD temperature and faults as well as current and voltage from MOSFETs/IGBTs. These GDs contain communication interfaces such as SPI for reconfiguration, verification, supervision, and diagnosis.

- **Protection features.** Gate Drivers usually include complementary circutis to provide additional protection features, such as:
  - *Miller clamp protection*: The Miller clamp function controls the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the off state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is turned on due to the C_{gc} capacitance.
  - *Under Voltage Lockout (UVLO):* This is key feature to ensure the system is protected in case of a bias supply failure. In isolated gate drivers, the voltage supply is provided at both the primary and secondary sides of the IC. During operation, if the power supply voltage drops and becomes lower than the UVLO detection voltage, UVLO brings the internal circuit into a semi-standby state to prevent malfunction. When the power supply voltage rises and becomes higher than the UVLO release voltage, UVLO is released and the operation restarts.
  - *Overvoltage lockout (OVLO):* This function protects the output side GD and external transistor from damagingly high supply voltages.
  - *Overcurrent (OC):* This protection is used to sense if the current of transistors is under overcurrent or shoot-through condition.
  - *Desaturation (DESAT) Short-circuit protection:* A short circuit protection (DESAT) ensures the protections of the power transistors during short-circuit. When the DESAT voltage goes up and reaches V_{DESAT} threshold, the output is driven low.
  - *Short circuit clamp:* Currents may be induced back into the gate-driver outs and CLAMP pins under short circuit events due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on power outputs and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.
  - *Thermal shutdown:* The power outputs are turned off when the GD junction temperature reaches a threshold.
  - *Overlap protection:* This prevents the two outputs (high-side/low-side) of a GD from going high simultaneously.
  - *Deglitch filter:* To increase the robustness of GD over noise transients and accidental small pulses on the input pins, i.e., IN+, IN–, RST/EN, a deglitch filter is designed to filter out the transients and ensure there are no faulty output responses or accidental driver malfunctions.
  - *Electrostatic discharge (ESD) capability:* Some GD adopts ESD based on diodes to protect GD-ICs and transistors. The diodes quickly absorb a large overvoltage (surge) and prevent it from being applied to other connected ICs and semiconductors.

There are many commercial models available for silicon and SiC devices. However, available GaN gate drivers are limited due to GaN switching requirements such as gate voltage and high-speed operation. Table 2.1 summarizes some commercial gate driver solutions compatible with GaN transistors used in industry applications for high-frequency and high-power applications.

Table 2.1 Commercial GDs compatible with GaN Transistors

Manufacturers	Models	Characteristics	Advantage	Drawbacks
Texas Instruments	• LM5113 • LMG1205	• Dual channel • Small propagation delay:28 ns • Protections: miller clamp, OVLO	• Galvanic Isolated • Advanced protections • Low cost • Small propagation delay:28 ns	• Limited functionalities • Non-isolation
	• UCC2751x	• Single channel • Protections: UVLO	• Small propagation delay:13 ns • Very low cost	• Limited functionalities • Non-isolation
SKYWORKS	• Si82XX	• Single/Dual channel • Isolated driver • Functionalities and protections: miller clamp, UVLO, OVLO, thermal shutdown, dead time control and overlap protection. • High voltage application: 1500 V_{rms} • Short circuit and thermal shutdown • EDS capability	• All functionalities and advanced protections	• High propagation delay: up to 140 ns
ANALOG DEVICES	• ADuM4121ARIZ • ADuM4121BRIZ	• Single channel • Isolated gate driver • Functionalities and protections: UVLO, OVLO, thermal shutdown, dead time control. • propagation delay:90ns	• All functionalities and advanced protections • Low cost	• High propagation delay: 90ns
	• MAX5048C	• Single channel	• Small propagation delay: 8ns • Very low cost	• Basic totem-pole • Non-functionalities and advanced functions • Non-isolation
BROADCOM	• ACPL-P346	• Single channel • 2.5 A maximum peak output current • UVLO protection • Isolated driver	• Low cost • Rail to rail output driver	• Limited functionalities • High propagation delay: up to 120ns
Infineon	• 1EDF5673K • 1EDF5673F • 1EDS5663H	• Single channel • Isolation:1.5 kV • EDS capability	• Low cost • High availability	• Limited functionalities
	• 2EDR8259H	• Dual channel • 5 A maximum peak output current • UVLO protection • Isolated driver		

As previously commented, GaN transistors can operate at high-speed transitions; therefore, very high-speed gate drivers are required to ensure the benefits of GaN. In addition, it is desired that a gate driver has as many functionalities as possible for protection. Regarding Table 2.1, gate drivers with many functionalities are commonly very slow, while simple gate drivers are commonly very fast drivers.

Some commercial drivers integrate advanced features; for example, the family models Si82XX are advanced GDs which combine many functions; however, they are very slow circuits which limit GaN transistor transition performance. In general, simple gate drivers are faster than advanced gate drivers. However, all commercial drivers, even for SiC MOSFETs, have limited capability to reduce overshoots and ringing issues. Even though some drivers have functions for adding circuitries and optimizing the GaN transitions, they cannot avoid the total issues, especially for high-power applications. Therefore, investigations of new gate-driving techniques are necessary to address oscillations and overshoot problems and increase GD performance when applied to WBG devices. The following sub-section presents an overview of the gate-driving techniques, particularly for GaN devices.

2.2 GATE DRIVING TECHNIQUES FOR WBG DEVICES

Wide Bandgap (WBG) devices are crucial for converters in new applications. As previously commented, several issues need to be addressed, especially to find solutions for improving the switching performance and reducing the oscillations and overshoot problems of SiC and especially GaN, which is an immature technology for high-power systems.

Optimising PCB layout is fundamental to reducing parasitic elements and their effects. Researchers have presented methods for designing PCB layouts to reduce parasitic inductances [7], [8], mainly the gate loop parasitic inductance and the power loop parasitic inductance (L_{loop}), which are critical for high-speed operation of the GaN [9], [10]. However, even if the inductance can be reduced, oscillations occur at higher voltages and frequencies. Conventional GD based on pull-up or pull-on resistors or two diodes and two resistances to control the GaN's turn-on and turn-off transition can improve device switching [9]. However, high-speed problems of GaN transistors are not entirely avoided.

Gate-driving techniques and circuits can improve the behaviour of GaN devices. In the literature, some GD concepts and ICs drivers presented for SiC MOSFETs could be adapted and used for GaN devices [11], [12]. However, particular features of the GaN transistors, such as lower gate voltage and higher speed operation, limit the gate driver systems available for SiC devices.

Gate-driving methods and GD circuits for GaN transistors have also been investigated and evaluated. Reported driving techniques include two-step [13], three-step [14], or multi-stage approaches [15], [16] which create gate voltage or current waveform profiles to control the turn-on and turn-off slopes and mitigate the high-speed GaN issues. Multi-stage gate drivers use low-power switches governed by a digital controller to change the gate resistance or voltage supplies to achieve different voltage or current profiles or patterns at the gate of the transistor.

Multi-stage gate drivers have been developed as monolithic systems integrated into a chip [14], [17], [18]. Monolithic drivers reduce the effects of stray inductance and circuit noise, and complex arrays of gate transistors can be combined to achieve high-level structures.

However, monolithic solutions are limited to specific applications and known loads, and the gate driver architecture cannot change once integrated.

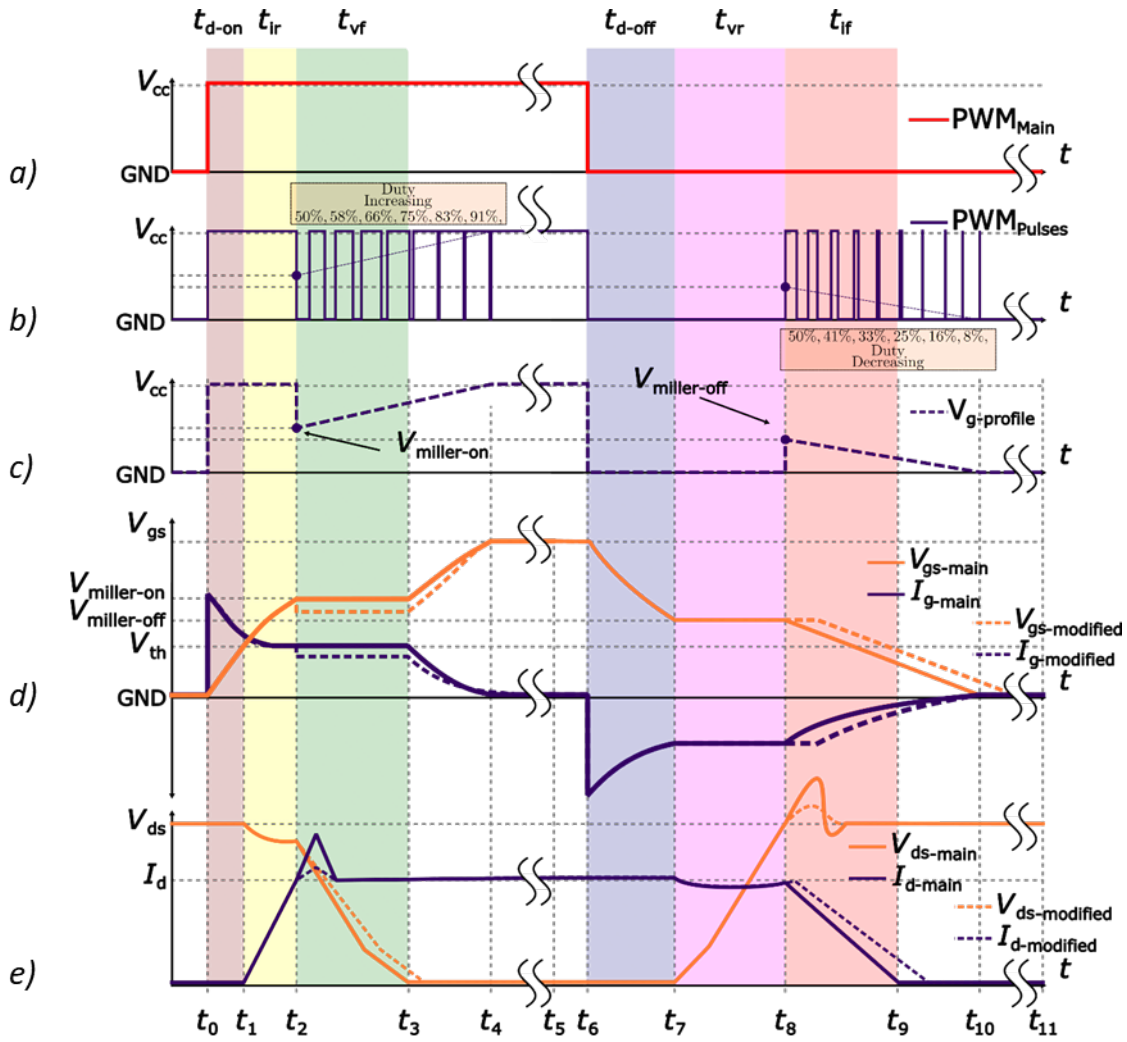
Gate-driving methods and circuits presented in the state-of-the-art have advantages and disadvantages. Generally speaking, the solutions presented can reduce overshoots and oscillations with acceptable transition performance. However, many gate drivers are limited to specific applications and low-voltage, low-power systems. Consequently, new gate-driving solutions must be investigated to improve GaN transitions, especially for high-power applications.

This deliverable investigates and evaluates a gate-driving approach for GaN power transistors, especially those used in RHODaS inverters.

3. GATE DRIVING APPROACH BASED ON HIGH-FREQUENCY PWM

3.1 GATE DRIVING CONCEPT

The gate driving approach involves shaping a custom gate voltage (V_g) profile by applying a variable high-frequency PWM inside the primary switching frequency PWM to control the energy applied at the turn-on and turn-off GaN transitions, as shown in Figure 3.1.



a) Original Gate-Voltage PWM; b) Modified Gate-Voltage high-frequency PWM; c) Expected Gate -Voltage profile; d) Vgs/Igs waveforms; e) Vds/Id waveforms

Figure 3.1. The gate-driving concept and waveforms representation

Ideally, the Vg profile (Figure 3.1 *c*, purple dotted line) is expected. However, this profile can be emulated in practice by varying the PWM at a high-frequency and given periods. For turn-on, variable PWMs from 0 to 50% could be generated, while PWMs from 50% to 0% could be generated for turn-off. The following sections will define the percentages and application periods of the variable PWMs.

The high-frequency PWMs are generated by an FPGA connected to a simple commercial totem pole circuit to supply the required current for the GaN power devices, as shown in Figure 3.2. This circuit includes the parasitic DUT GaN model, inductive load, and critical inductances as L_{loop}.

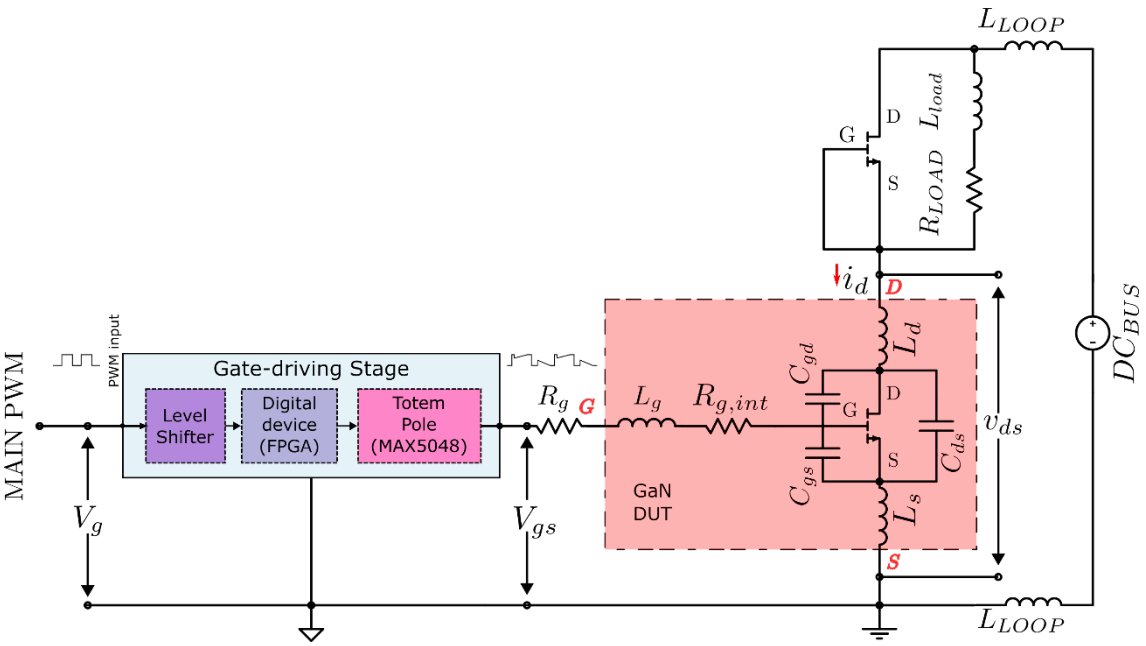


Figure 3.2. Power circuit for active gate driving design and validation

3.2 GATE DRIVING PROCESS

Considering Figure 3.1 in the first half of the PWM period, the V_g profile starts just as the conventional PWM for regular charging the input capacitances up to the Miller plateau at t_2. At this point, V_g falls to Miller Voltage (V_{Miller}) to limit the gate current (I_g); from this point, the V_g increases until the gate-source voltage (V_{gs}) reaches the nominal V_{cc} at t4, then shapes a slope signal. From this time, V_g remains at V_{cc} until the first half of the PWM period ends.

It is important to note that the V_{Miller} of the V_{gs} with standard PWM (Figure 3.1 *d*, orange waveform line) defines the inflexion point for shaping the V_g profile. When the V_g profile is applied, the new V_{gs} (Figure 3.1 *d*, doted waveform in Figure 3.1) will cause a lower level of V_{Miller} due to the drop voltage of R_g. As the V_{Miller} with new V_{gs} is lower than conventional V_{gs}, the gate driving would warranty the expected results.

Considering again Figure 3.1, in the second half of the PWM period, the V_g profile (Figure 3.1 *d* orange line) remains just as the conventional PWM for regular discharging of the output capacitances until the Miller plateau ends (t_8). At this point, V_g rises to V_{Miller} to restrict the I_g; from this point, the V_g goes until the V_{gs} reaches the nominal lower voltage (GND) using a slope as a reference. From this time, V_g remains at GND until the second half of the PWM period ends.

With the defined V_{gg} profile, the drain current (I_d) and drain-source voltage (V_{ds}) should behave better, with lower turn-on and turn-off transition oscillations, as shown in Figure 3.1 *e*).

3.3 GATE DRIVING CRUCIAL PARAMETERS DEFINITION

Figure 3.1 shows that the V_{miller} and transition stages are essential for the gate-driving definition. Therefore, these parameters must be known or calculated to achieve the expected V_g profile.

The Miller voltage (V_{Miller}) is a voltage reference for the star of the high-frequency PWM, which should be calculated or defined. Manufacturers always provide the Vth, and often, they proportionate the $Vmiller$ as constant and the same value for turn-on and turn-off. In practice, V_{miller} can change due to system dynamics and could be different for turn-on and turn-off transitions. Nevertheless, V_{miller} has been defined in the literature [19] and can be approximated by (1) and (2).

$$V_{miller-on} = \left(\frac{Vth\, G_m R_g C_{GD} + I_L R_g C_{GD} + V_g (C_{GD} + C_{DS})}{(1 + G_{fs} R_g) C_{GD} + C_{DS}}\right) \quad (1)$$

$$V_{miller-off} = \left(\frac{V_{th} G_m R_g C_{GD} + I_L R_g C_{GD}}{(1 + G_m R_g) C_{GD} + C_{DS}}\right) \quad (2)$$

Where the capacitances C_{GD} and C_{DS} can be obtained by $C_{iss} = C_{gs} + C_{gd}$, $C_{oss} = C_{ds} + C_{gd}$ and $C_{rss} = C_{gd}$. The capacitances C_{iss}, C_{oss}, C_{rss} can be found in the datasheets by the manufactures.

3.4 TRANSITION TIMES

There are various methods to obtain the transition times. The manufacturer in the datasheets provides approximate turn-on and turn-on transition times; however, they are defined as an ideal case study without considering circuit parasitic elements. This simple model differs from the final application, where various parasitic elements are present, such as the transistor loop inductances, power loop inductances and the printed circuit parasitic elements. In the literature, models often fit equations and models to determine the energy and losses of transistors, seeking values closer to real behavior [19], [20], [21]. Table 3.1 shows the summary of the equations to approximate the time stages.

Table 3.1. Equations to determine the time transitions of GaN transistor

Stage	Times by calculations
t_{don}	$t_{d-\text{on}} = (R_g \text{Ciss}) \ln\left(\frac{V_{\text{gs}}}{(V_{\text{gs}} - V_{\text{miller}}) - V_{\text{TH}}}\right)$
t_{ir}	$t_{\text{ir}} = (\,5 * (R_g\,(C_{\text{gd1}} + C_{\text{gs}}))\,) - t_{d\_\text{on}}$
t_{vf}	$t_{\text{vf}} = R_g * \left(\frac{Q_{\text{gd}}}{V_{\text{DS}}}\right) * \left(\frac{V_{\text{DS}}}{V_{\text{gs}} - V_{\text{miller}}}\right)$
t_{end-on}	$t\_\tau_2 = 5 * (R_g\,(C_{\text{gd2}} + C_{\text{gs}}))$
$t_{\text{on-total}}$	$\text{Ton\_total} = t_{d-\text{on}} + t_{\text{ir}} + t_{\text{vf}} + t\_\tau_2$
t_{doff}	$t_{d-\text{off}} = \tau_2 = 5 * (R_g\,(C_{\text{gd2}} + C_{\text{gs}}))$
t_{vr}	$t_{\text{vr}} = R_g * \left(\frac{Q_{\text{gd}}}{V_{\text{DS}}}\right) * \left(\frac{V_{\text{DS}}}{V_{\text{miller-off}}}\right)$
t_{if}	$t_{\text{if}} = \sqrt{(g_m * L_d) * (R_g * C_{\text{gd}})\left(\frac{V_{\text{miller}} - V_{\text{th}}}{V_{\text{miller}}}\right)}$
$t_{end-off}$	$t\_\tau_1 = R_g C_{\text{iss}} \ln\left(\frac{V_{\text{th}}}{0.01 * V_{\text{th}}}\right)$
$t_{\text{off-total}}$	$\text{Toff\_total} = t_{d-\text{off}} + t_{\text{vr}} + t_{\text{if}} + t\_\tau_1$

4. GATE DRIVING EVALUATION AT OPEN LOOP CONTROL

The gate-driving concept presented in Section 3 has been developed and validated by simulation in the LTspice framework using the circuit shown in Figure 4.1, based on the circuit defined in Figure 3.2. The used LTspice simulation model comprises commercial models of GaN transistors and totem pole driver components provided by manufacturers.

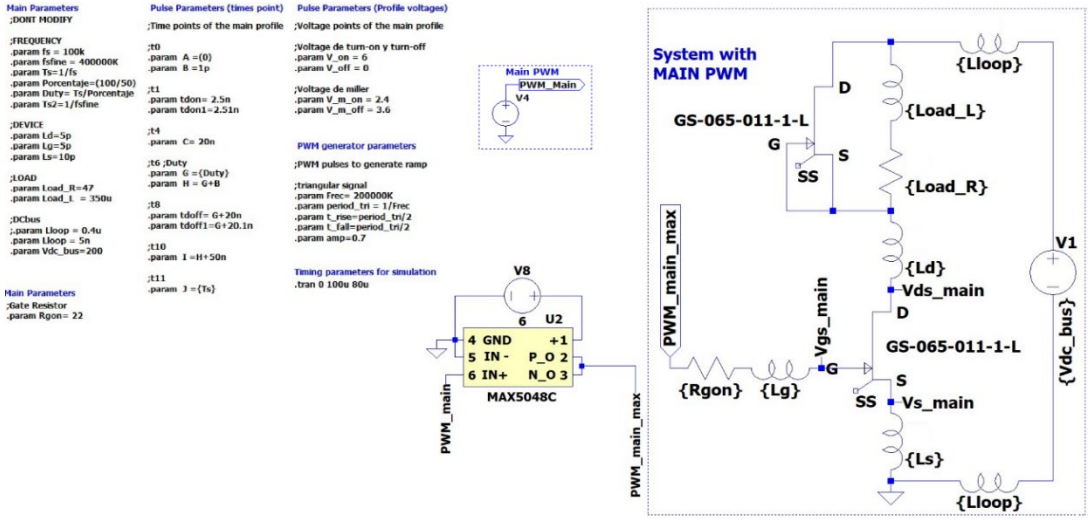


Figure 4.1. LTspice model for gate-driving evaluation

The GaN transistor model GS-065-011-1-L by GaN System was used for all analyses. Meanwhile, the totem pole driver LTspice model used was the IC MAX5048C from Analog Devices manufacturer. Table 4.1 shows GaN transistor and totem pole driver parameters taken from the datasheet.

Table 4.1. GaN Transistor and totem-pole main specifications

Component	Characteristics	Symbol	Value	Units
GaN Transistor GS-065-011-L	*Drain to source voltage*	V_{DS}	650	[V]
	Continuous drain current	I_{DS}	7.2	[A]
	Gate-to-source voltage	V_{GS}	-10 to 7	[V]
	Drain-to-source Resistance	$R_{DS(on)}$	150	*[mΩ]*
	Turn-On Delay	$T_{D(on)}$	5	[ns]
	Rise Time	t_R	5	[ns]
	Turn-Off Delay	$T_{D(off)}$	8	[ns]
	Fall Time	t_F	10	[ns]
Totem-pole Driver MAX5048C	*Voltage operating range*	V+	+ 4 to 14	[V]
	Maximum Output current	I_{out}	7	[A]
	Propagation delay	$T_{D\text{-}ON}/T_{D\text{-}OFF}$	8	[s]
	Rise time	t_R	5	[ns]
	Fall time	t_F	4	[ns]

The LTspice GaN model considers critical parasitic capacitances and inductances obtained from papers, datasheets, and application notes. In addition, it includes other parameters such as VMiller, Vth, and Vgs, which are crucial for calculating the time transition and voltage set points for gate drive applications. Table 4.2 shows the main parasitic elements, key voltages, and resistances for time transition determination.

Table 4.2. GaN transistor parameters and parasitic elements used for calculations and simulations

Parameters	Value	Parameters	Value
C_{ds}	19.6 pF	L_d	5 nH
C_{gd}	0.4 pF	L_g	5 nH
C_{gs}	69.6 pF	L_s	10 nH
C_{iss}	70 pF	L_{loop}	5 nH
C_{oss}	20 pF	L_{load}	350 uH
C_{rss}	0.4 pF	R_{load}	47 Ω
Q_{GD}	0.7 nC	R_g	10 Ω
C_{ds}	19.6 pF	V_{gs}	6 V
V_{miller}	3 V	$V_{miller\text{-}on}$	2 V
V_{th}	1.7 V	$V_{miller\text{-}off}$	1.6 V

The parameters $V_{miller\text{-}on}$ and $V_{miller\text{-}off}$ in Table 4.2 have been obtained by using Equations 1 and 2. As previously commented, these voltages define the start points of variable PWMs at GaN transitions. On the other hand, Table 4.3 shows the electrical specifications to perform the simulations.

Table 4.3. GD Simulation Assessment Specifications

Parameter	Value
V_{dc} bus [V]	200
Maximum Load current [A]	4
Switching frequency [kHz]	100
duty cycle of primary PWM [%]	50

4.1 TIME STAGE EVALUATIONS

Calculations were performed to obtain the time steps required for the gate control definition considering Figure 3.1, which are t2, t4, t8 and t10. The time steps were calculated using Table 3.1 and the specifications shown in Table 4.1, Table 4.2 and Table 4.3. Furthermore, simulations were developed to measure these same times. Table 4.4 compares the equivalent time steps obtained by analysis and simulations.

On the other hand, Figure 4.2 shows the time transitions. The color codes are those defined in Figure 3.1

Table 4.4. Transition times results comparison

	Stage	Times by calculations	Times by simulations
Turn-on	$\boldsymbol{t_2} = t_{\text{don}} + t_{\text{ir}}$	3.77 ns	3.61 ns
	$\boldsymbol{t_4} = t_2 + t_{\text{vf}} + t_{end-on}$	14.58 ns	34.01 ns
Turn-off	$\boldsymbol{t_8} = t_{\text{doff}} + t_{\text{vr}}$	13.14 ns	25.42 ns
	$\boldsymbol{t_{10}} = t_8 + t_{\text{if}} + t_{end-off}$	21.14 ns	50.43 ns

As shown in Table 4.4, the time steps have the same order of magnitude, although there are some differences in the values that define the new shape of the PWM pulse, which are 52% in the case of (t_{don} + t_{ir}) and 3% for the time (t_{vf} + (t_3-t_4).

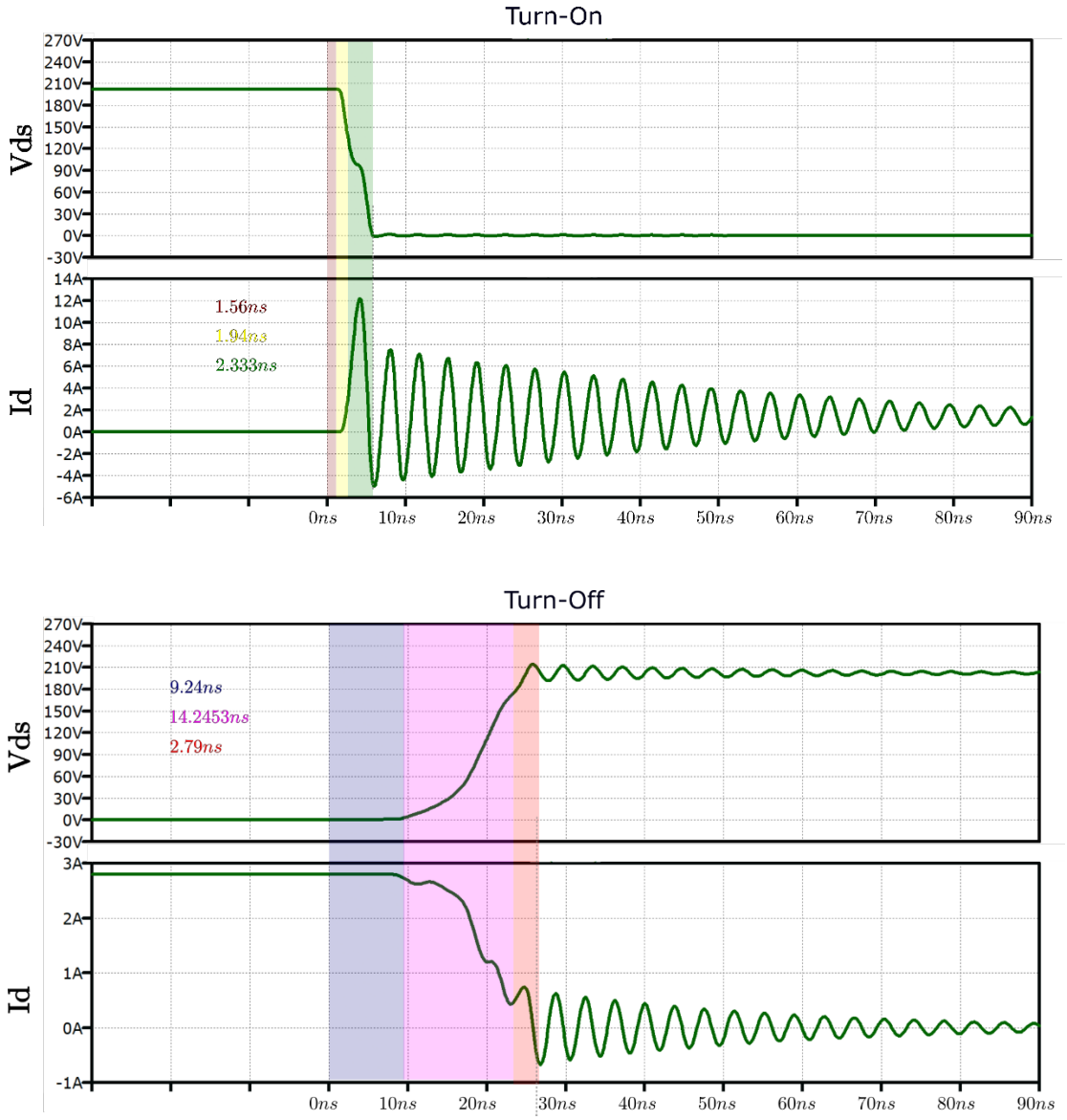


Figure 4.2. Representation of time transitions of GaN by simulations

As expected, the time transitions of the GaN devices is very short, which limits the operating range to actuate on the PWM gate signal, to generate the adjustable duty cycle trend. However, However, using a high frequency PWM pulses conformer it is still possible to modify the voltage profile of the applied PWM gate signal.
By using LTspice to simulate the gate driving it is possible determining the pulse quantities and the periods of each pulse (see Figure 3.1 b). The obtained results are analyzed in the next section.

4.2 GATE-DRIVING EVALUATION BY MEANS SIMULATIONS

The expected profile was defined in LTspice, and the gate-driving concept was evaluated based on the conditions defined in Table 4.3 and the transition times obtained in Table 4.4. Simulations were performed and results of advanced gate driving was compared with conventional gate driving based on a single R_g to analyze the performance advantages.

The gate driving was evaluated in open loop and at different operating points in both turn-on and turn-off transitions. Figure 4.3 and Figure 4.4 show the results obtained. Ideal Vg profile and duty-adjust pulses were simulated for observing the effect of the gate driving. The ideal Vg profile was generated by using the PWL LTspice tool.
On the other hand, to generate and adjust the duty of the high-frequency pulse sequence and achieve the expected profile, the standard PWM was considered a reference at the switching frequency of the GaN transistors, 100 kHz, in these simulations. Then, to generate the high-frequency PWM, a triangular signal (carrier signal at 200 MHz) was compared with the desired profile (reference signal) to obtain the desired duty-adjusted pulse sequence.

The color codes in Figure 4.3 and Figure 4.4 are as follows: Green color, original waves without modifying the PWM gate driver pattern; Blue color, theoretical waves when applying a modified PWM gate drive pattern; Red color, resulting waves after applying the developed PWM concept to the PWM gate drive pattern.

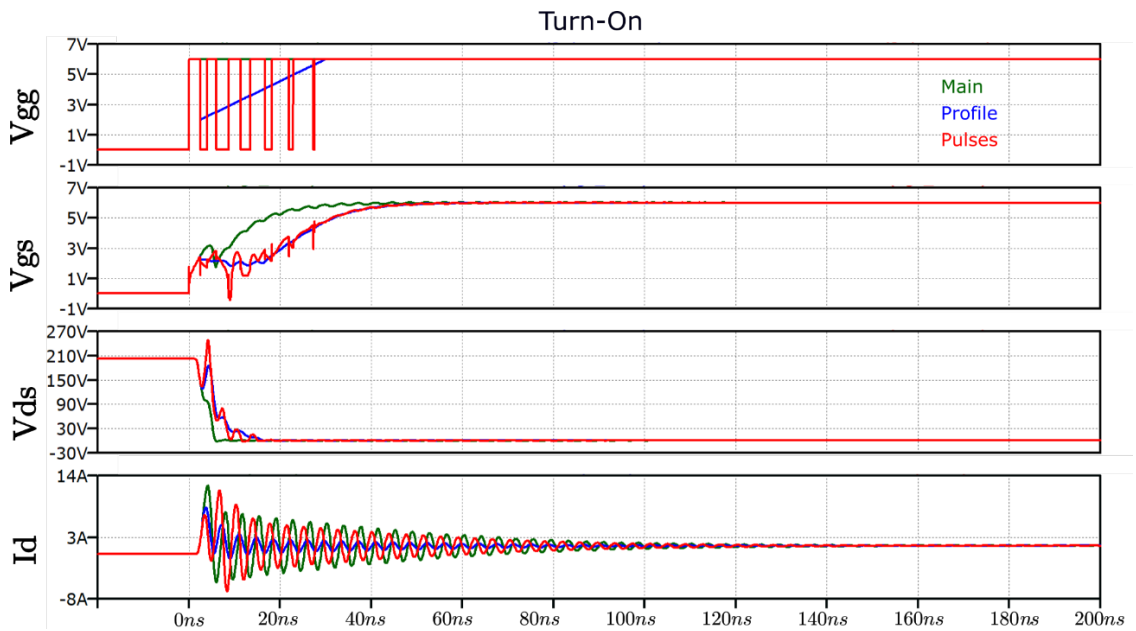


Figure 4.3. Currents and voltages of GaN under gate-driving method at turn-on.

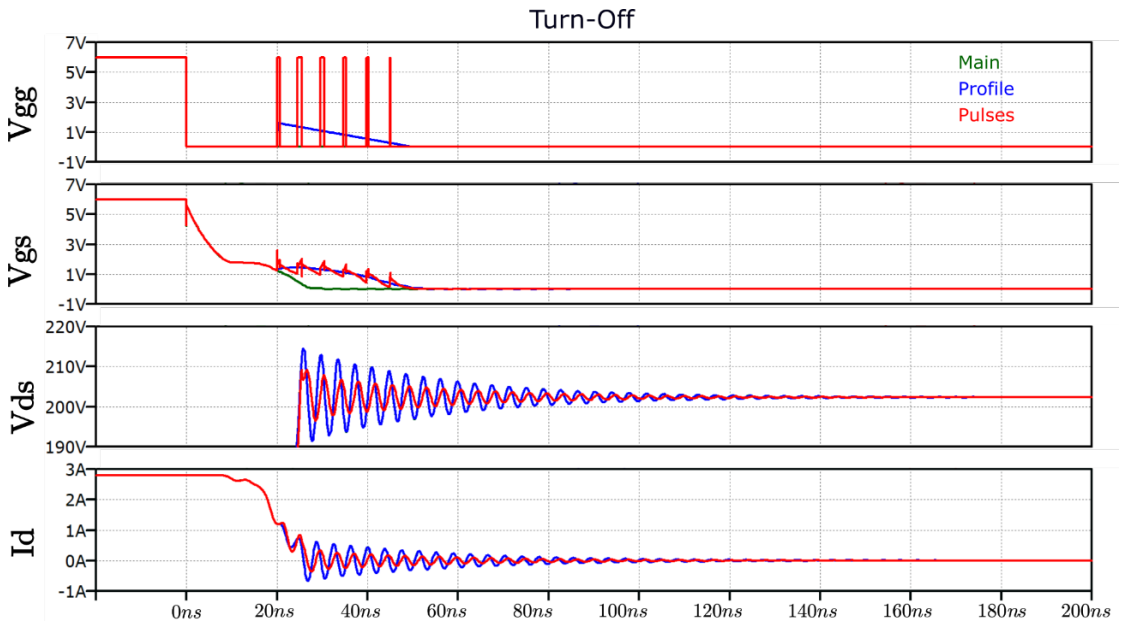


Figure 4.4. Currents and voltages of GaN under gate-driving method at turn-off

From Figure 4.3 and Figure 4.4, both for turn-on and turn-off, it can be concluded that advanced gate driving can reduce the overshoots and amplitude of the oscillations without a significant increase in delays at the transitions. To verify the performance, a quantitative comparison of the GaN power losses and overshoots between the gate-driving approach and conventional gate driver was performed. Table 4.5 shows the power losses. Meanwhile, Table 4.6 shows the overshoot percentages.

Table 4.5. Power losses comparison

Type	**P_{total} (W)**	**$P_{sw\text{-}on}$ (W)**	**$P_{sw\text{-}off}$ (W)**	**P_{cond} (W)**
Conventional GD	0.7419	0.2359	0.1390	0.3569
Proposed GD	0.8272	0.3082	0.1532	0.3565

Table 4.6. Overshoots comparisons

	Turn-on overshoot reduction (%)	**Turn-off overshoot reduction (%)**
V_{DS}	15	2,8
I_D	40,29	13

The comparison shows that the proposed gate control technique has slightly higher switching losses than the conventional method. For instance, if we consider $Pc_{onduction}$ = 0.3569 W, with the conventional gate driver the losses are P_CL_{osses} = 0.2359 W + 0.1390 W = 0.7419 W. On the other hand, losses resulting of applying the proposed gate driver method are P_PL_{osses} = 0.3082 W + 0.1532 W + 0.3565 W.

Based on this calculation, the estimated losses are 11.49%, indicating the effectiveness of this method. Considering the total device losses, these increase by 11.49%. However, the reduction of the peak current I_d and voltage V_{ds} is 15% and 40.29%, respectively, which reduces the risk of overcurrent and overvoltage stress and breakdown of the circuit in high-power industrial applications. This conclusion is particularly important for the use of GaN devices in high-voltage-high-power applications, as is the case of the RHODaS project, due to the limited maximum ranges in voltages and currents available in the current generation of GaN transistors.

5. GATE DRIVING EXPERIMENTAL EVALUATION

5.1 GATE DRIVING PROTOTYPING AND SETUP

The developed gate driver is evaluated in the laboratory to investigate its feasibility in real conditions. As shown in Figure 5.1, a setup based on the circuit presented in Figure 3.2 was mounted. This setup uses GaN devices GS-065-011-1-L, Totem-pole Driver MAX5048C, and an FPGA Artix 7 on a board by Digilent to generate the duty-adjustable high-frequency pulses to conform the PWM gate drive pulses.

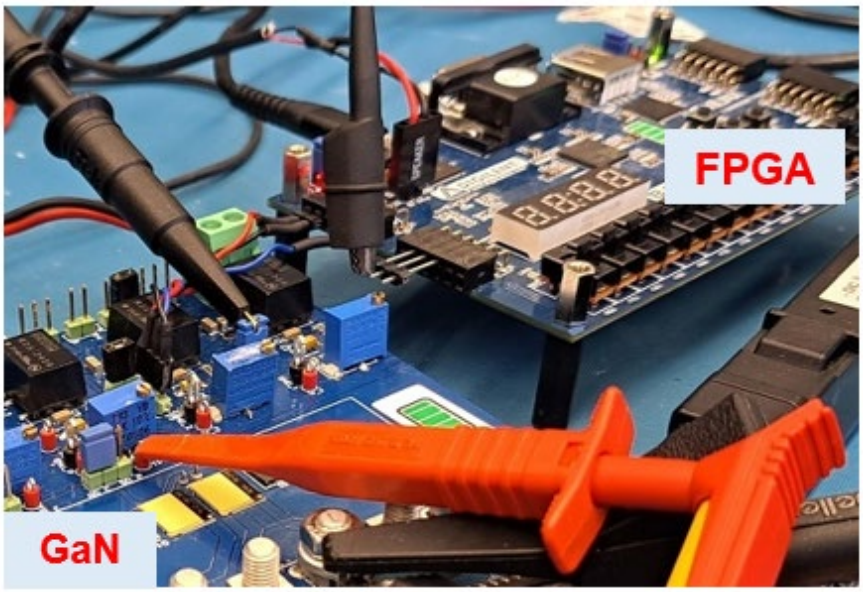


Figure 5.1. Gate driver experimental set-up

The electrical parameters shown in Table 4.3 were used for the laboratory analysis of the gate driving. The tests were performed in two stages. In the first stage, the duty-adjustable high-frequency pulses was generated in the FPGA to analyze the correct generation of pulses. After that, the gate drive PWM pulses were modified to obtain the expected profiles. In the second part, the power stage was installed, and the advanced gate driving was applied to the transistor for voltage and current behavior evaluation.

5.2 GATE-DRIVING ON FPGA IMPLEMENTATION

As is shown in Figure 5.2, the duty adjust pulse sequences in the FPGA were created by using a frequency divider (MMCM or PLL), which is generated by using a phase shift stage with six clocks synchronized at the same sampling frequency. The output signal of the phase shifter enters the duty generator stage, which is based on programmable logic blocks to generate different duty cycles.

In parallel, a custom profile is at the lookup table (LUT) connected to the desired profile (referenced to the PWM standard) enters the programmable logic blocks stage. Finally,

with a MUX and an additional programable logic block called a pulse generator, the duty-adjust pulse sequence is achieved for turn-on and turn-off of the GaN transitions.

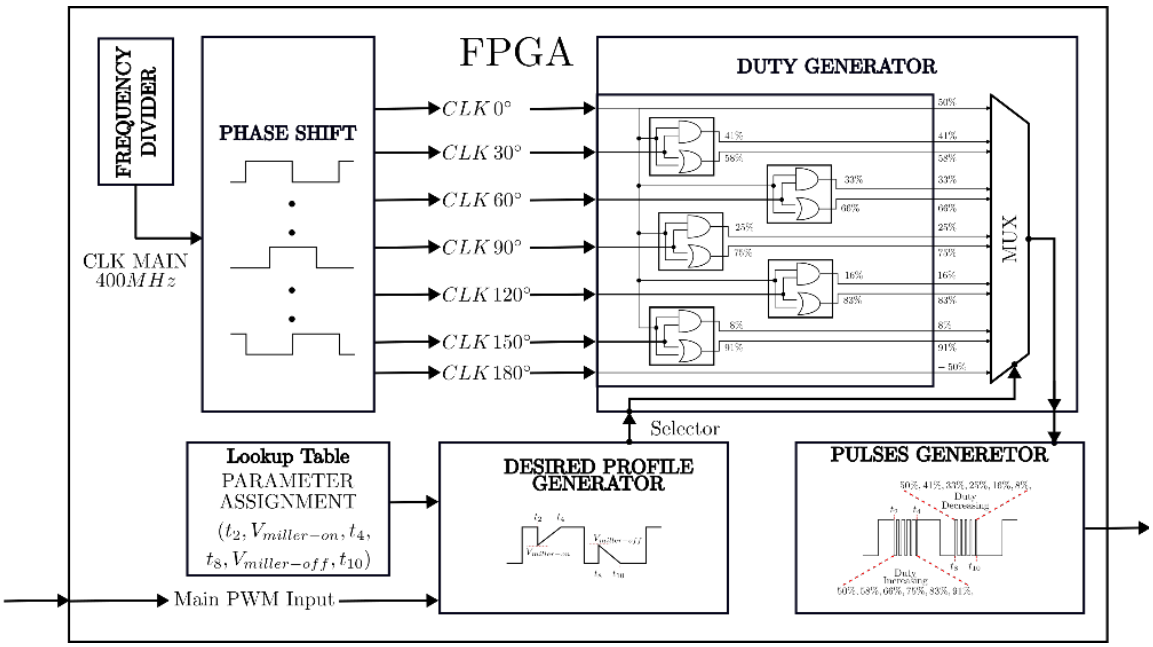


Figure 5.2 Artix 7-FPGA architecture and concept for gate driving pulses generation

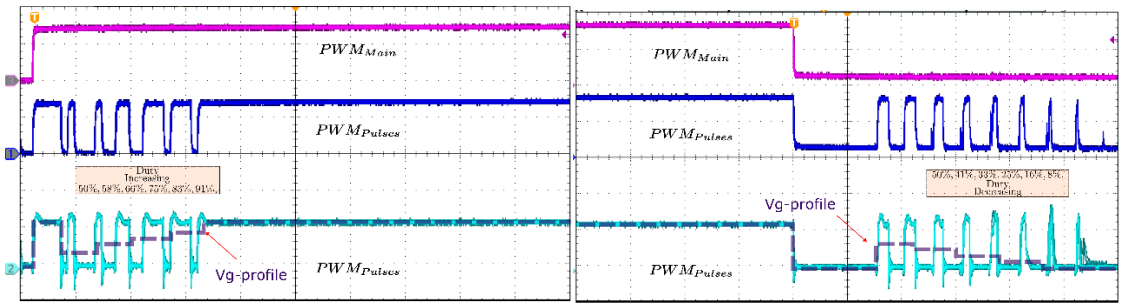


Figure 5.3. FPGA and totem pole driver outputs; High frequency PWMs and expected Vg profile

As is shown in Figure 5.3, it was possible to generate the duty-adjustable high-frequency pulses; however, the FPGA Digilent Basic board has limitations concerning the physical clock, which has a frequency of 100 MHz, which limits the period of the duty-adjustable pulses. Applying the frequency divider shown in Figure 5.2, it was possible to achieve a resolution with a minimum step of 2.5 ns. With this step time, it was possible to prove the gate-driving method.

5.3 EXPERIMENTAL RESULTS AND CIRCUIT'S CHALLENGES

To compare the behavior of the transistors', conventional gate drivers based on a single resistance were applied, like the simulation previously presented. conventional gate driver (a) and the new gate driving method (b).

The developed gate was applied to a GaN transistor mounted in an experimental circuit with a scheme as shown in Figure 3.2. The loading and control parameters are presented in Table 4.2 and Table 4.3. The I_d and the V_{ds} were measured on the resulting circuit.

To compare the behavior of the transistors, conventional gate drivers based on a single resistor were applied, as was done also in the simulation presented above. Figure 5.4 shows the V_{ds} and I_d with the conventional gate driver (a) and the new gate control method (b). An impressive reduction in I_d peak can be seen at the turn-on switching, without significantly affecting the rest of the on/off parameters.

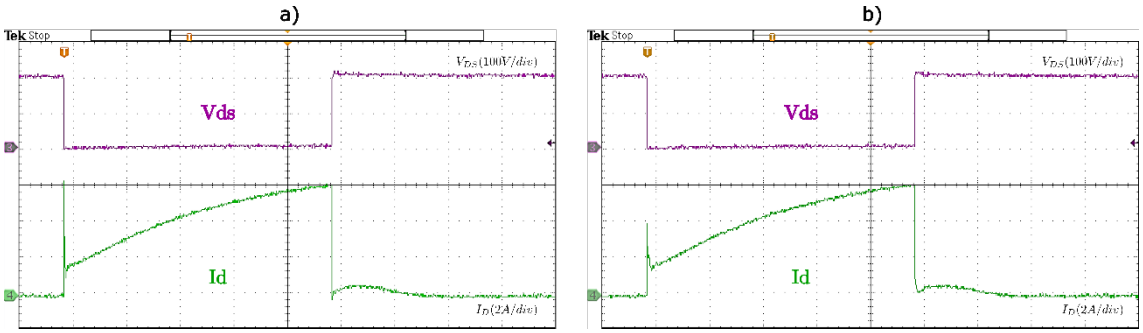


Figure 5.4. Gate driving comparison on one operating cycle. V_{ds}=200V, I_d 4 A maximum and f_s=100kHz.

As shown in Figure 5.4, experimental measurements demonstrate that the new gate drive technique can reduce the overshoot current I_d. Figure 5.5 and Figure 5.6 show details of the on-off transitions of the conventional (main) gate drivers and the (modified) gate drive technique.

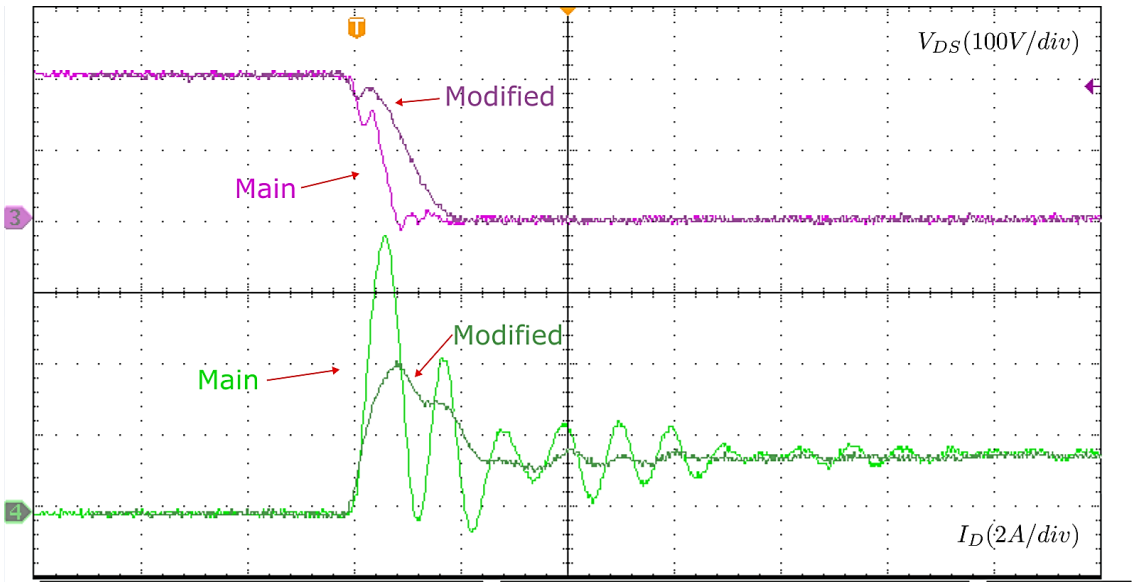


Figure 5.5. Gate driver comparison at turn-on transition. V_{ds} = 200 V, I_d =4 A and f_s=100kHz

Figure 5.5 shows that the gate control technique results in a better turn-on transition. The overshoot can be reduced to just 50% and the ringing can also be significantly reduced without a significant increase in transition delay.

Figure 5.6 shows the voltage overshoot limitation that is achieved with the proposed method at the turn-off transition, which is reduced by 12.5% while also reducing the voltage ringing.

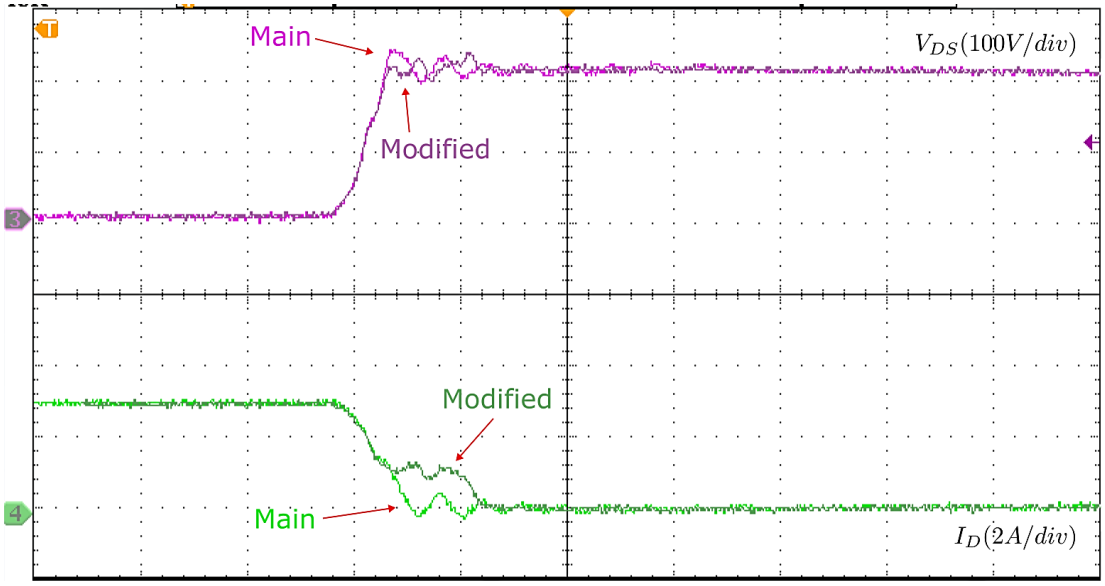


Figure 5.6. Gate driver comparison at turn-off transition. V_{ds}=200 V, I_d = 4 A and f_s=100kHz.

Analyzing the results of the tests performed, it can be said that the proposed gate control presents poorer characteristics and more limitations in the turn-off transition than in the turn-on transition. The main reason is the low resolution allowed by the FPGA. For the period in which the adjustable cycles are required, only four adjustable pulses can be generated with the available FPGA used in the experiments. The resulting 2.5 ns pulse period prevents the voltage level from forming the expected V_g profile.

This problem could be solved by using an FPGA with a higher frequency operation and applying a larger number of adjustable pulses based on the duty, as shown by the simulations.

It should be noted that for the turn-on stage, four pulses were sufficient to achieve the V_g profile within the active operation area of the GaN; then, spikes and oscillations were reduced.

5.4 CHALLENGES AND LIMITATIONS OF GATE DRIVING APPROACH

A gate control design based on high duty-frequency pulse sequences as designed presents many challenges when applied to GaN transistors. The main drawback is the number of pulses allowed by the FPGA for the short transition times of GaN. To achieve a better Vg profile, an FPGA with an associated clock higher than 100 MHz and an operating frequency higher than 400 MHz could improve the results.

On the other hand, high-speed components, such as totem-pole gate drivers, are required to apply the presented gate control technique. In addition, the gate control technique must be integrated with advanced gate drivers, as presented in Table 2.1, to cover as many features as possible.

Gate control was evaluated using an open loop concept, where the I_d current is considered to be kept almost constant at its nominal value during converter operation, for example, in electrochemical battery charging systems.

Automation of this technique for any use case can be achieved by adapting the switching time calculations shown in Table 3.1 to the actual Id current. This solution, which would

include a feedback to read the I_d current, would improve the dynamics of the Gate Driver operation, but would increase the complexity of the solution and the integration costs may be very high.

The problem is mitigated, however, if an integrated Gate Driver is built that incorporates all the necessary elements in a compact design: I_d current reading, switching time calculation block, and pulse shaper with high-frequency hardware.

The results show, however, that the presented solution, even with constant I_d current steady state operation, offers substantial improvements over currently available solutions for high voltage applications.

Additionally, this type of gate control can also be applied to SiC devices, which with a longer transition time than GaN could operate with lower FPGA frequencies and slower, less expensive auxiliary components.

6. GATE DRIVING FOR RHODAS WBG CONVERTER

The developed gate control can be applied to the WBG devices used in the RHODaS project, which were described in deliverables D2.1 and D2.3. Figure 6.1 shows the integration of the developed gate driver with the GaN devices of the low (15kW) and high (150kW) power T-Type inverters, whose specifications are shown in Table 6.1.

It should be noted that, for reasons of compactness and electrical safety of operation, the RHODaS high-power converters use compact GaN power modules (Half-Bridge) from Infineon that integrate the GD circuit inside (deliverable D2.3), forming a holistic system that limits the application of additional gate drivers. However, gate control can be easily applied to GaN devices of the low-power T-Type converter, where the necessary connections have already been included to be used in the experimental tests of this converter with the developed gate driver.

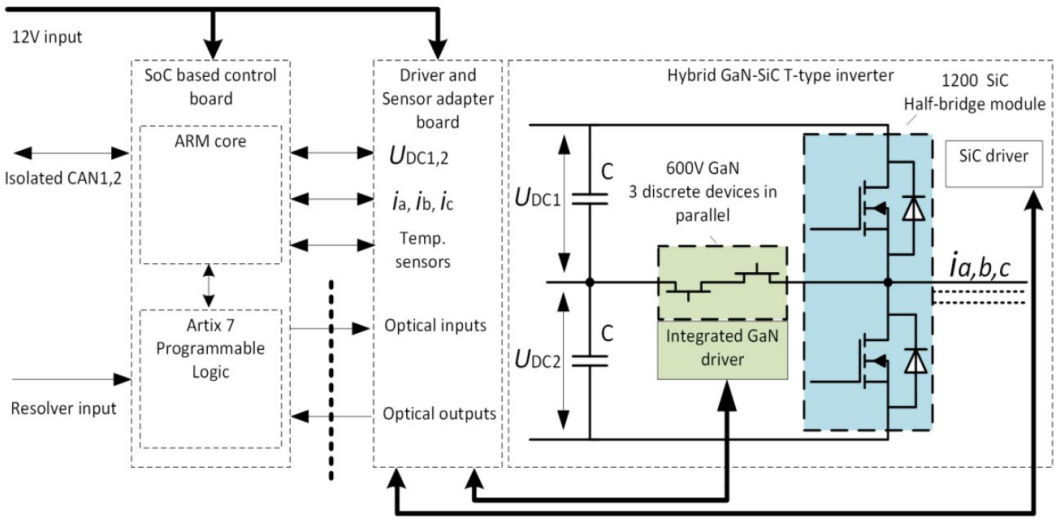


Figure 6.1. The overall structure of the high-power inverters of RHODAS

Table 6.1. RHODAS converter specifications

Parameter	Low-power converter	High-power converter
Power density	---	100 kW/L
Maximum efficiency	> 98 %	
DC bus voltage	800 V	1000 V
Rated power	10 kW	150 kW
Maximum power	15 kW	250 kW
Max. swtiching frequency	50 – 100 kHz	
Rated current (rms)	12 A	150 A
Peak current (rms)	18.75 A	250 A
Topology	T-type (GaN+SiC)	3 GaN e-HEMTs in parallel

Figure 6.2 shows how gate control for GaN transistors can be implemented in the RHODAS low-power converter. Regarding D2.3, currently, the low-power converter uses a commercial gate driver, ADuM4121ARIZ, from Analog Devices, whose main specifications are shown in Table 6.2.

The gate control technique uses MAX5048C, whose specifications are presented in Table 4.1. The MAX5048C could be tailored to meet the power supply voltage and currents and outputs that will be required for RHODAS devices, presenting faster dynamic ranges.

By this way, RHODAS's lower power converter can be experimentally used to evaluate the improvements in the switching of the GaN devices that can be achieved with the developed gate driver in different use cases. For instance, the impact of applying the advance gate driving developed on the different modulation strategies presented in D2.3 could be evaluated.

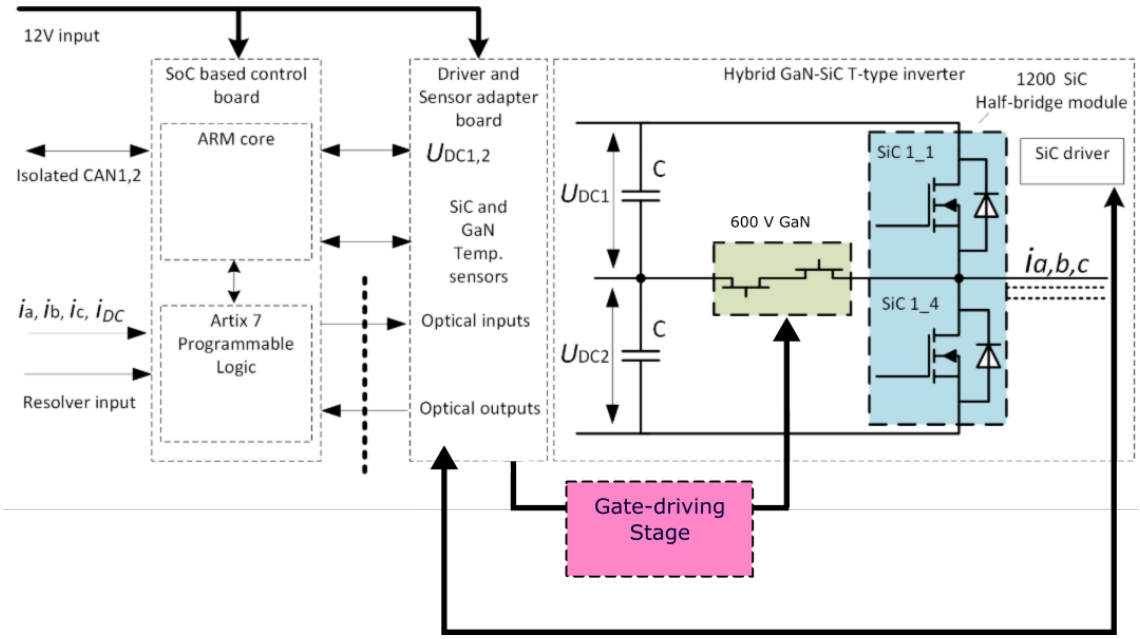


Figure 6.2. A gate-driving adaptation approach

Table 6.2. ADuM4121ARIZ gate driver specifications

Component	Characteristics	Symbol	Value	Units
ADuM4121ARIZ	*Voltage operating range*	*V+*	+2 to 35	[V]
	Output current max	I_{out}	2	[A]
	Propagation delay	$T_{D\text{-}ON}/T_{D\text{-}OFF}$	53	[s]
	Rise time	t_R	42	[ns]
	Fall time	t_F	53	[ns]

7. CONCLUSION AND NEXT STEPS

7.1 CONCLUSIONS

This paper analyzes some commercial gate drivers available for GaN and SIC devices and proposes an approach for gate control of WBG devices. The new gate control technique is based on a high duty frequency pulse sequence tunable, validated by simulation and laboratory tests at 200 V DC bus and 100 kHz switching frequency.

The results presented in this paper show that this advanced gate control can improve the transition of GaN transistors despite their inherent high-speed operation. Gate control can reduce overshoots and spikes, especially the I_d current, which can be reduced to 50%, and minimize oscillations. The gate control approach was somehow very limited in reducing the V_{ds} voltage overshoots due to the limitation of the available FPGA used for this work. However, improvements in turn-off could be achieved using FPGAs with better characteristics.

Although advanced gate control techniques are difficult to implement in GaN transistors due to the high-speed response and short delay components required to achieve effective operation in the GaN active region, this report has demonstrated the feasibility of this particular control technique under real experimental conditions.

The gate control development resulted in a conference paper, which will be presented in September at ECCE Europe 2024.

7.2 NEXT STEPS

The next step in the development of this technology, born within the framework of the RHODaS project, is to apply the developed gate control to the power modules of the low-power T-type converter used in RHODaS, in order to analyze the improvements that can be achieved in this converter technology and to establish the contributions.

Once the validation of the gate control in the low-power T-type converter is concluded, further step consists in the development and integration of an active gate driver based on this adjustable duty frequency high-pulse technology. The resulting active gate control could be implemented in higher voltage and current converters, even in high-power, high-voltage half-bridge converters for DC/DC conversions.

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